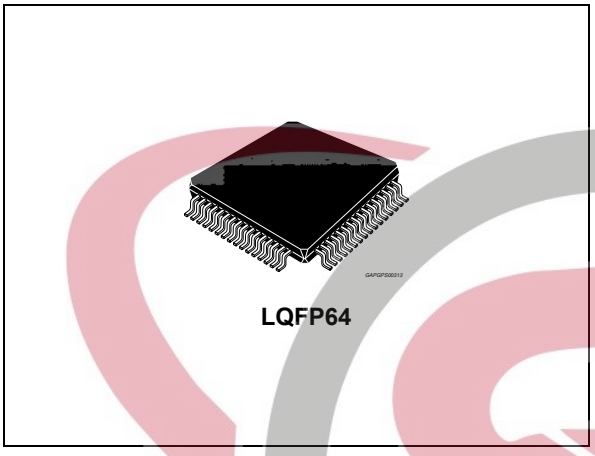
TDA7706M

Highly integrated tuner for AM/FM car-radio

Datasheet - production data



LQFP64

Features

- FM, AM and weather band reception
- Fully integrated VCO for world tuning
- High performance PLL for fast RDS system
- Integrated AM-LNA and PIN diodes
- Automatic self alignment for FM front-end pre-selection filter and image rejection
- Integrated IF filters with high selectivity, dynamic range and adaptive bandwidth control
- Drift-free Digital-IF signal processing with high performance
- RDS demodulation with group and block synchronization
- High performance stereo decoder with noise-blanker
- Digital interface for HD Radio™ reception with digital audio blending
- MuSICA Algorithm for Multipath noise reduction
- Fully programmable DSP core
- I^2C bus-controlled
- I^2S input/output digital audio interfaces
- Single 5 V supply
- LQFP64 package

Description

The TDA7706M highly integrated tuner is a high/performance AM/FM tuner IC for car-radio applications, suitable for HD Radio™ reception.

It contains mixers and IF amplifiers for AM, FM and WX, fully integrated VCO and PLL synthesizer, IF- processing including adaptive bandwidth control, stereo-decoder, RDS decoder, and digital interfaces for external HD Radio™ decoding on a single IC.

AM/FM IBOC or DRM base band filtering is available in parallel to standard analog reception.

The proprietary MuSICA algorithm greatly enhances the FM reception quality under multipath conditions.

The utilization of digital signal processing results in numerous advantages: very low number of external components, very small space occupation and easy application, very high selectivity due to digital filters, high customization possibility through software control, automatic alignment and a powerful DSP for custom processing.

Table 1. Device summary

Order code	Package	Packing
TDA7706M	LQFP64 (10x10x1.4mm)	Tray

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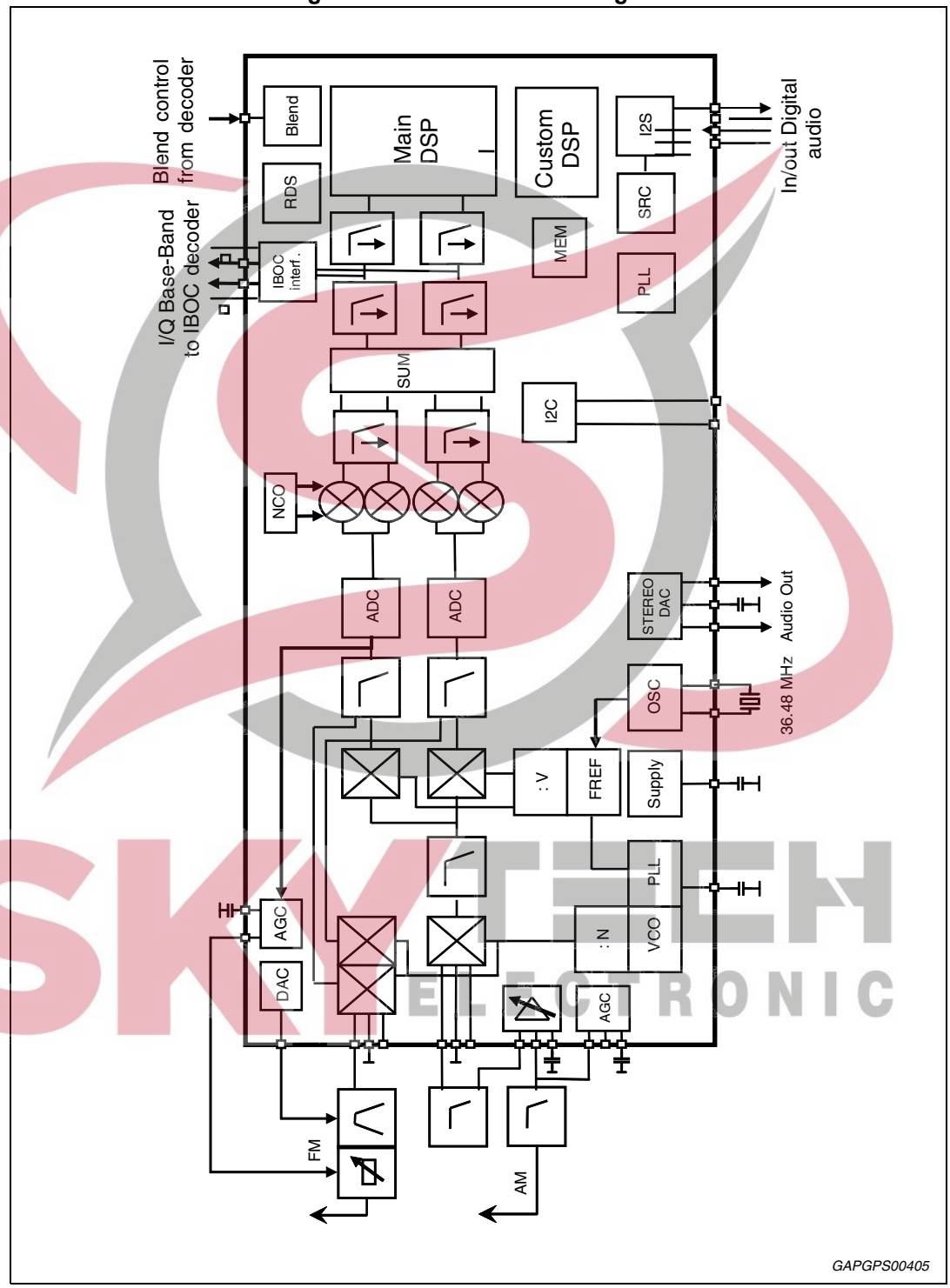
1.1 Block diagram

Figure 1. Functional block diagram



1.2 Pin description

Figure 2. Pin connection (top view)

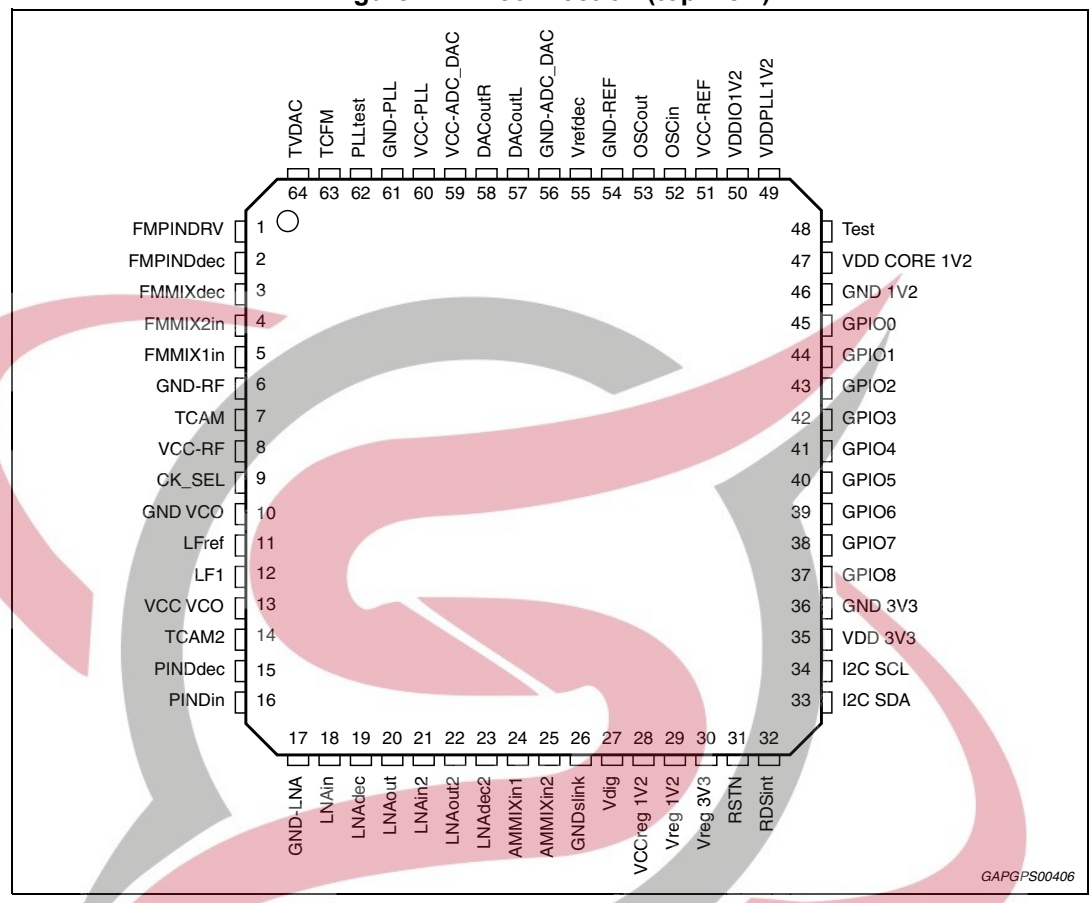


Table 2. Pin description

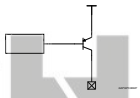
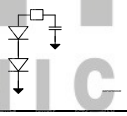
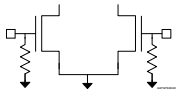
Pin	Pin name	I/O	Function	Description	Equivalent circuit
1	FMPINDRV	Out	FM	FM PIN diode driver output	
2	FMPINDdec	In		Integrated FM PINdiode decoupling	
3	FMMIXdec	-		FM RF signal ground	
4	FMMIXin2	In		FM mixer input 2	
5	FMMIXin1	In		FM mixer input 1	
6	GNDRF	-	-	RF power ground	-

Table 2. Pin description (continued)

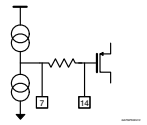
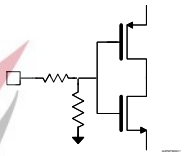
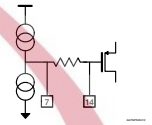
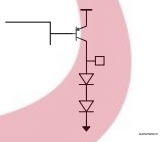
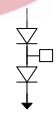
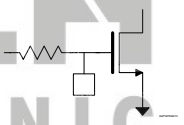
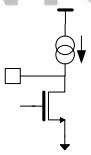
Pin	Pin name	I/O	Function	Description	Equivalent circuit
7	TCAM	-	-	AM AGC time constant	
8	VCCRF	In	-	RF 5 V supply	-
9	CK_SEL	In	-	Master/Slave clock operation select	
10	GNDVCO	-	VCO	VCO ground	-
11	LFref	-		Loop filter reference	-
12	LF1	-		Loop filter output	-
13	VCCVCO	In		VCO 5 V supply	-
14	TCAM2	-		AM AGC 2nd order time constant	
15	PINDdec	-	AM pin diode	AM AGC internal PIN diode decoupling	
16	PINDin	-		AM AGC internal PIN diode input	
17	GNDLNA	-	AM LNA	AM LNA ground	-
18	LNAin	In		AM LNA input	
19	LNAdec	-		AM LNA decoupling	
20	LNAout	Out		AM LNA output	-
21	LNAin2	-		AM LNA input 2nd stage	-

Table 2. Pin description (continued)

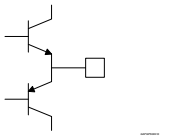
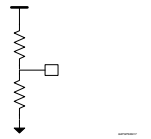
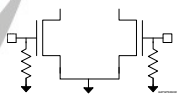
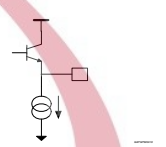
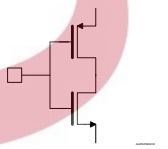
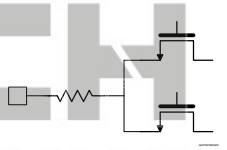
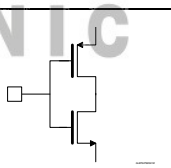
Pin	Pin name	I/O	Function	Description	Equivalent circuit
22	LNAout2	-	AM LNA	AM LNA output 2nd stage	
23	LNAdec2	-		AM LNA decoupling 2nd stage	
24	AMMIXin1	In	AM mixer inputs	AM mixer input 1	
25	AMMIXin2	In		AM mixer input 2	
26	GNDSLINK	-	Supply, ground and reset	Internal inter-IC communication bus ground	-
27	Vdig	In		Front-end digital 5 V supply	-
28	VCCreg1V2	In		Internal 1.2 V regulator 5 V supply	-
29	REG1V2	Out		Internal 1.2 V regulator output	
30	Vreg3v3	Out		Internal 3.3 V regulator output	
31	RSTN	In		Reset (low active) Pull-up 50 kΩ to 3.3 V IO supply	
32	RDSint	Out		RDS interrupt output Pull-down 50 kΩ to ground	-
33	I2CSDA	In/Out	I2C interface	I2C bus data Pull-up 50 kΩ to 3.3 V IO supply	
34	I2CSCL	In		I2C bus clock Pull-up 50 kΩ to 3.3 V IO supply	
35	VDD3V3	In	-	IO ring (3.3 V) supply	-
36	GND3V3	-	-	IO ring (3.3 V) supply	-

Table 2. Pin description (continued)

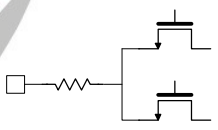
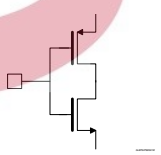
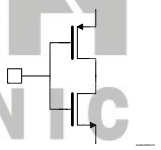
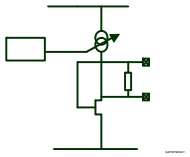
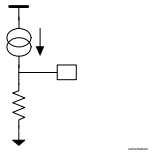
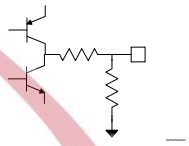
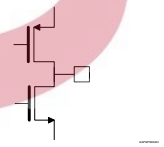
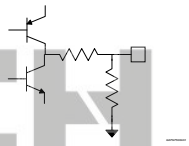
Pin	Pin name	I/O	Function	Description	Equivalent circuit
37	GPIO8	In/Out	HD Radio connectivity/ Audio output I2S interface	SAI clk Pull-down 50 kΩ to ground, SINE_3V3_LIN pad	
38	GPIO7	In/Out		Audio SAI word-select Pull-down 50 kΩ to ground, SINE_3V3_LIN pad	
39	GPIO6	In/Out		Audio SAI data-output Pull-down 50 kΩ to ground, SINE_3V3_LIN pad	
40	GPIO5	In/Out		Audio SAI data-input Pull-down 50 kΩ to ground, SINE_3V3_LIN pad	
41	GPIO4	In/Out		SAI Base-Band clock Pull-down 50 kΩ to ground, SINE_3V3_LIN pad	
42	GPIO3	In/Out		SAI Base-Band word-select Pull-down 50 kΩ to ground, SINE_3V3_LIN pad	
43	GPIO2	Out		SAI Base-Band I data Pull-down 50 kΩ to ground, SINE_3V3_LIN pad	
44	GPIO1	Out		SAI Base-Band Q data Pull-down 50 kΩ to ground, SINE_3V3_LIN pad	
45	GPIO0	In		HD blend Pull-down 50 kΩ to ground	
46	GND1V2	-	-	DSP core ground	-
47	VDD core 1V2	In	-	DSP core 1.2 V supply	-
48	Test	In	-	Test Mode Pull-down 50 kΩ to ground	
49	VDDPLL1V2	In	-	Digital PLL 1.2 V supply	-
50	VDDIO1V2	In	-	Internal inter-IC communication 1.2V supply	-
51	VCC-REF	In	-	Front-end reference frequency and regulator 5 V supply	-

Table 2. Pin description (continued)

Pin	Pin name	I/O	Function	Description	Equivalent circuit
52	OSCin	In	Oscillator	Crystal oscillator input	-
53	OSCout	Out		Crystal oscillator output	
54	GND-REF	-	-	Front-end reference frequency and regulator ground	-
55	Vrefdec	-	-	3.3 V Bias generation decoupling	
56	GND-ADC_DAC	-	DAC	IFADC and audio DAC ground	-
57	DACoutL	Out		Audio output left	
58	DACoutR	Out		Audio output right	
59	VCC-ADC_DAC	In		IFADC and audio DAC 5 V supply	-
60	VCC-PLL	In	PLL	Tuning PLL 5 V supply	-
61	GND-PLL	-		Tuning PLL ground	-
62	PLLtest	Out		PLL Test output	
63	TCFM	-	-	FM AGC time constant	
64	TVDAC	Out	-	Tuning voltage output	-

2 Function description

2.1 FM - mixers

The FM Image Rejection mixer has two single ended inputs, selectable through software. They are designed for achieving best performance both in case of a passive tuned preselection and for a passive fixed band-pass preselection without tuning for lower cost applications.

The input frequency is down-converted to very low IF with high image rejection.

The tuned application is supported by an 8-bit tuning DAC. The alignment of the DAC is performed automatically on-chip.

2.2 FM - AGC

The programmable RFAGC senses the mixer input to avoid overload.

When the RFAGC threshold is reached, the PIN diode output is activated in order to attenuate the incoming RF signal

The PIN diode driver is able to drive external PIN diodes with up to 15 mA current.

The time constant of the FM AGC is defined by the combination of an external capacitor and internal currents. There are two programmable attack and decay time constants.

2.3 AM - LNA

The integrated AM LNA feature is integrated with low-noise and high IIP2 and IIP3. The gain of the LNA is controlled by the AGC. The maximum gain is set with an external resistor, typically 26 dB with 470 ohm.

2.4 AM - AGC

The programmable AM RFAGC senses the mixer inputs and controls the internal PIN diodes and LNA gains.

Firstly the LNA gain is reduced by about 10 d B, and then the PIN diodes are activated to further attenuate the signal.

The time constant of the 2^{nd} order AM AGC LPF is defined by both external components and programmable internal currents.

2.5 AM - Mixers

The image rejection mixer has two AM inputs selectable via software. It easily supports low-cost applications for extended frequency bands like short-waves.

The input frequency is converted to low IF with high image rejection.

2.6 IF A/D converters

A high performance IQ-IFADC converts the IF signal to the digital domain for subsequent digital signal processing.

Two fully differential, continuous-time Sigma-Delta (ΣΔ) IF-ADCs are used for both the 'I' path and the 'Q' path. For each IFADC, two fully differential input nodes are fed with an input signal having a bandwidth up to 325 kHz. This fully differential design provides good suppression of even-order harmonics. For complex filtering, the input signals of the 'I' path and the 'Q' path have a 90 degree phase shift. The IFADC sampling frequency is 36.48 MHz.

2.7 Audio D/A converters

A CD-quality (>100dB DR) stereo DAC provides the left/right audio signals after IF processing and stereo-decoding by the DSP. In presence of an external HD Radio decoder the DAC outputs the high quality audio resulting from the decoding of the HD Radio transmissions.

2.8 VCO

The VCO is fully integrated without any external tuning component. It covers all the FM frequency bands including EU, US, Japan, East-Europe, Weather-Band and the AM-bands including LW, MW and SW. Its center frequency is approximately 2.7 GHz.

2.9 PLL

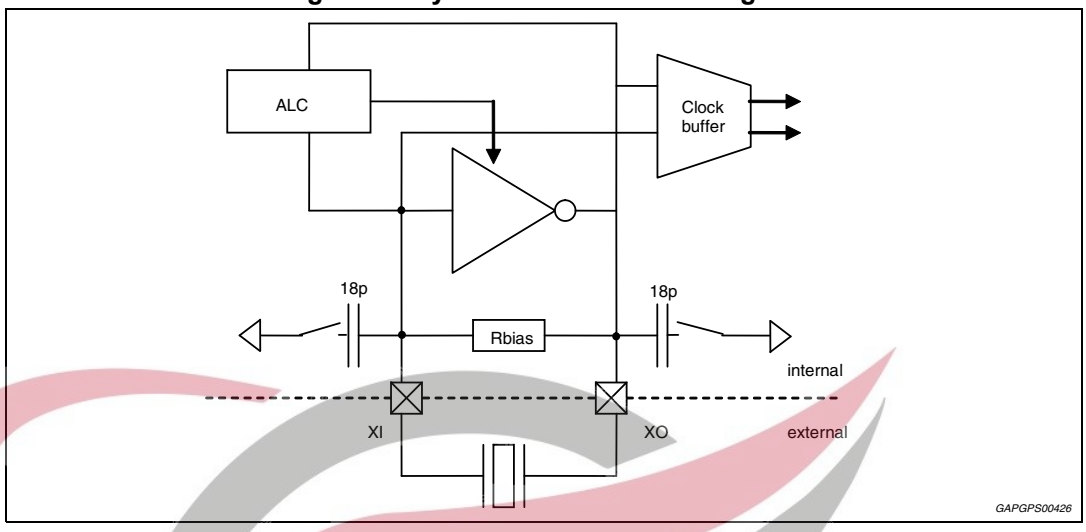
2.9.1 Tuner PLL

The very high-speed tuning PLL is able to settle within about 100 µs for fast RDS applications. The frequency step can be as low as 5 kHz in FM and 500 Hz in AM.

2.10 Crystal oscillator

The device works with a 36.48 MHz fundamental tone crystal. The oscillator block diagram is shown in *Figure 3*. On the PCB the crystal must be connected as close as possible to the chip oscillator input and output pins of the chip. The internal load capacitance together with pin and pad capacitance is optimized for fundamental tone crystal units at 36.48MHz. It is not recommended to put any additional external load capacitors. By suitably configuring pin #9 (CK_SEL), the device can be operated as either a clock master or a clock slave. If pin 9 is left open or tied to GND, the device is configured as clock master (typical operation mode). In case the device is configured as clock slave, pin 9 needs to be connected to 5V. Then the crystal oscillator is switched off and the device expects a crystal equivalent signal on the OSCout/OSCin pins.

Figure 3. Crystal oscillator block diagram



2.11 DSP

The TDA7706M embeds two DSP cores for high computational power and achievable customization. The first DSP and its hardware accelerators take care of all the tuner digital signal processing. The main program is fixed in ROM. Control parameters are copied to RAM and they are accessible and modifiable there, thus allowing a parametric performance optimization. The first DSP core performs:

- digital down-conversion of IF
- bandwidth selection with variable controlled bandwidth
- FM and AM noise blanking
- FM/AM demodulation with soft-mute, high-cut, weak signal processing and quality detection
- FM stereo decoding with stereo-blend
- RDS demodulation including error correction and block synchronization with generation of an RDS interrupt for the main µP
- Autonomous control of RDS-AF tests
- Self-alignment of pre-selection tuning

The second DSP is totally free for custom processing implementation. The second (customizable DSP) can interact with the main DSP by tapping the signal at the access points as shown in the *Figure 4* below.

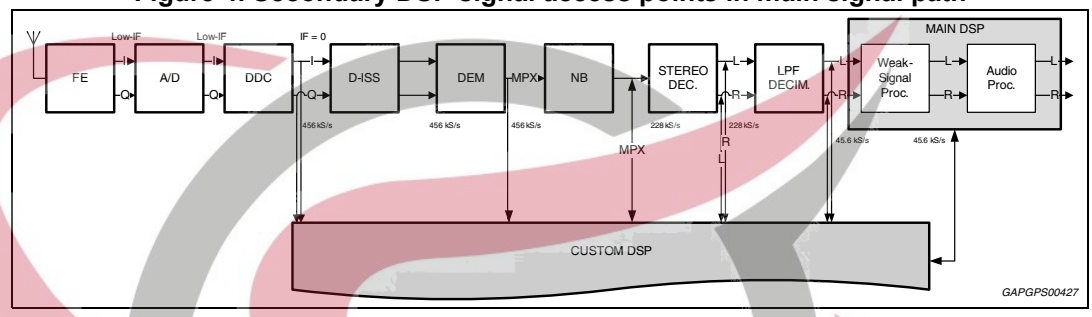
Table 3. Main DSP resources

Resource	Size	Unit	Word-length (bits)
Data Memory (XRAM)	2048	Kword	24
Data Memory (YRAM)	2048	Kword	24
Program memory (RAM)	4096	Kword	32
Program memory (ROM)	16384	Kword	32
Max Processing power	116	MIPS	-

Table 4. Custom DSP resources

Resource	Value	Unit	Word-length (bits)
Data Memory (XRAM)	2048	Kword	24
Data Memory (YRAM)	8192	Kword	24
Program memory (RAM)	8192	Kword	32
Program memory (ROM)	4096	Kword	32
Max Processing power	116	MIPS	-

Figure 4. Secondary DSP signal access points in main signal path



2.12 Multipath reduction

The TDA7706M is equipped with an FM multipath noise reduction system in addition to the traditional weak signal processing. The algorithm, called MuSICA, assures a substantially improved reception performance in presence of distortion originating from multipath.

2.13 GPIO - general purpose IO interface pins

The IC has several IOs tasked for connectivity to an external HD-radio/DRM decoder and/or to I^2S audio sources and destinations.

GPIO0-8 (pins 37 to 44) are driven by a special buffer that has been especially developed to allow reduced disturbance originating from activity on the digital lines. This bidirectional buffer is based on a TTL Schmitt trigger receiver and a slew-rate controlled driver with programmable cut-off frequency and current capability.

Typical configurations of GPIOs for both analog and digital-HD reception are indicated in *Table 5*; for the suggested configuration all the slew-rate controlled pads are programmed with a 10 MHz cut-off frequency:

Table 5. Suggested GPIO direction and driving capability

Pin	Direction (HD on)	Direction (HD off)	Driving capability	
			5pF	10pF
37	IN	IN		X
38	IN	IN		X
39	OUT	OUT		X
40	IN	IN		X

Table 5. Suggested GPIO direction and driving capability (continued)

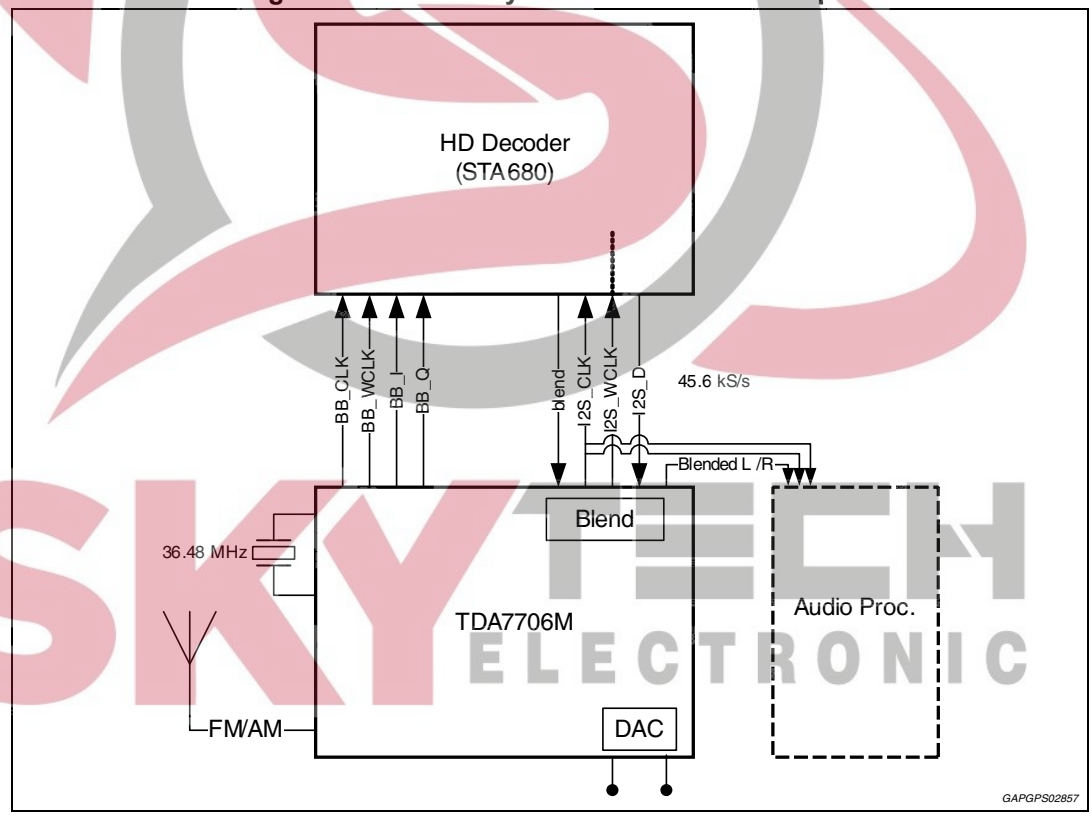
Pin	Direction (HD on)	Direction (HD off)	Driving capability	
			5pF	10pF
41	OUT	OUT	X	
42	OUT	IN		X
43	OUT	IN	X	
44	OUT	IN	X	

In case a different GPIO configuration is used, it is recommended to supply TDA7706M with an externally regulated 3.3 V source.

2.14 HD Radio connectivity

The HIT2 complies with HD Radio interface specifications as per Ibiquity's "RX_SSS_1108 HD Radio power efficient RF-IF and peripheral processing (power RIPP) specification", thus providing an external HD Radio decoder with I/Q base-band signals and receiving the decoded digital audio from it, as shown in *Figure 5*.

Figure 5. HD Radio system architecture example



The complex baseband signal of an IBOC or DRM transmission is sent to the external decoder using the dedicated digital output interface SAI_BB. The SAI_BB supports the modes shown in both *Figure 6* and *Figure 7*. Timing information for the protocols shown in both *Figure 6* and *Figure 7* is detailed in *Table 6* and *Table 7*.

Figure 6. SAI_BB waveforms (normal mode)

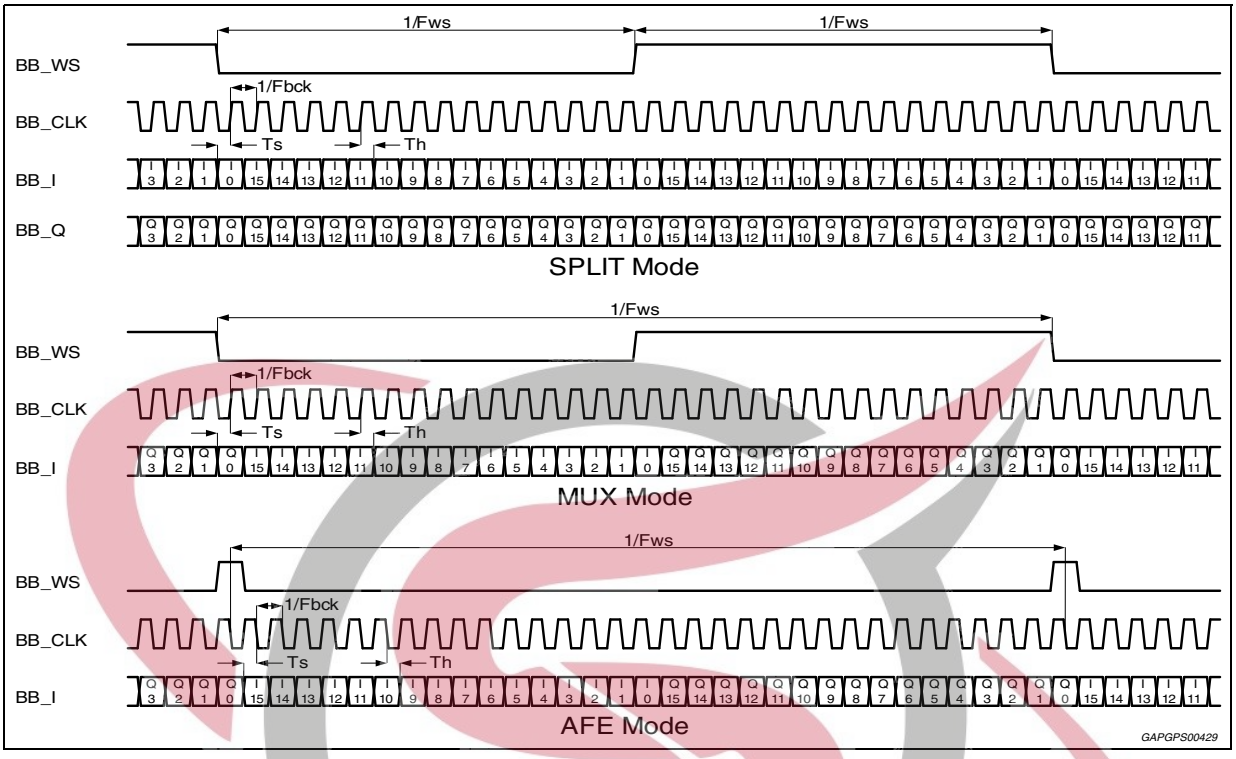


Table 6. SAI_BB timing values (normal mode)

Symbol	Parameter	Rate					Unit
Fpll	PLL clock	332.8	345.6	451.584	466.944	245.76	MHz
Fws	Word strobe	650 (332.8/512)	675 (345.6/512)	882 (451.582/512)	912 (466.944/512))	48 (245.76/5120)	KHz
Fbclk	Bit clock in SPLIT mode	10.4 (332.8/32)	10.8 (345.6/32)	14.112 (451.584/32)	14.592 (466.944/32)	0.768 (245.76/320)	MHz
Fbclk	Bit clock in MUX mode	20.8 (332.8/16)	21.6 (345.6/16)	28.224 (451.584/16)	29.184 (466.944/16)	1.536 (245.76/160)	MHz
Fbclk	Bit clock in AFE mode	20.8 (332.8/16)	21.6 (345.6/16)	28.224 (451.584/16)	29.184 (466.944/16)	1.536 (245.76/160)	MHz
Ts	Data setup time (min)	5	5	5	5	5	ns
Th	Data hold time (min)	5	5	5	5	5	ns

Figure 7. SAI_BB waveforms (burst mode)

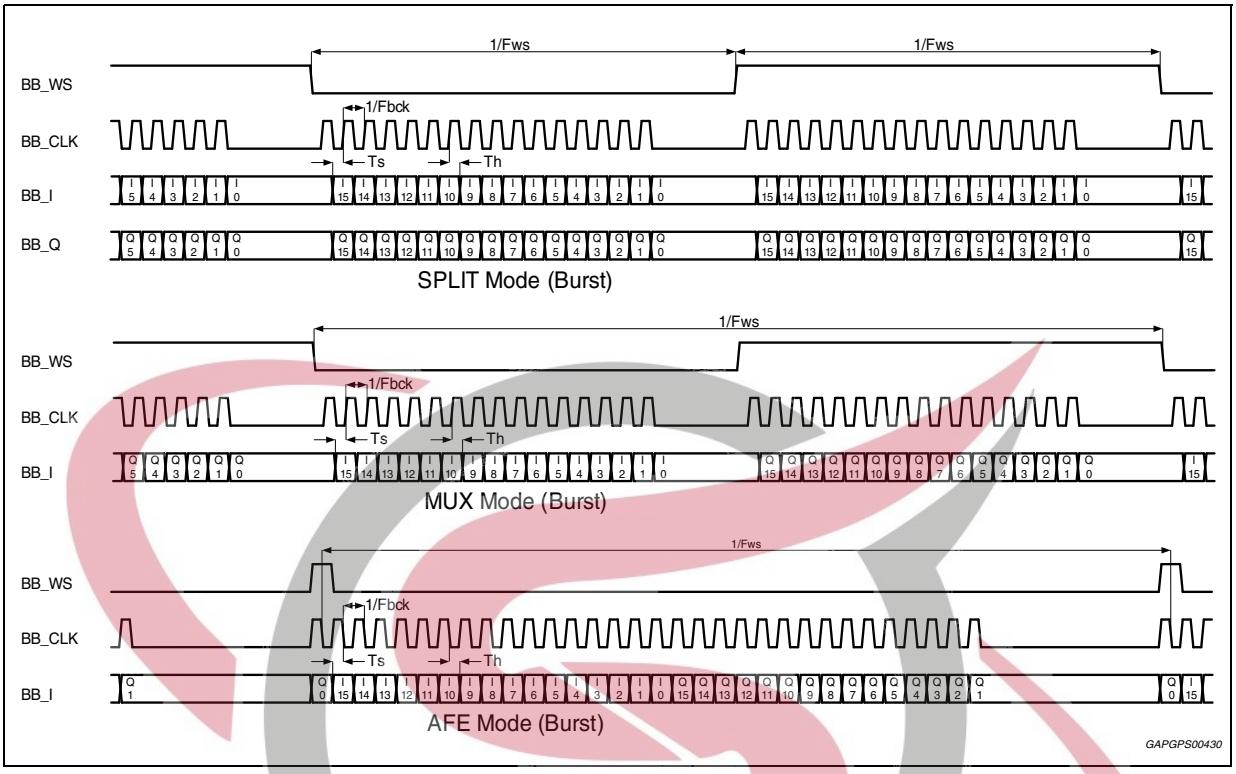


Table 7. SAI_BB timing values (burst mode)

Symbol	Parameter	Rate					Unit
Fpll	PLL clock	332.8	345.6	451.584	466.944	245.76	MHz
Fws	Word strobe	650 (332.8/512)	675 (345.6/512)	882 (451.582/512)	912 (466.944/512))	48 (245.76/5120)	KHz
Fbclk	Bit clock in SPLIT mode	332.8/n (n=16/32)	345.6/n (n=16/32)	451.584/n (n=16/32)	466.944/n (n=16/32)	245.76/n (n=160/320)	MHz
Fbclk	Bit clock in MUX mode	332.8/n (n=8/16)	345.6/n (n=8/16)	451.584/n (n=8/16)	466.944/n (n=8/16)	245.76/n (n=80/160)	MHz
Fbclk	Bit clock in AFE mode	332.8/n (n=8/16)	345.6/n (n=8/16)	451.584/n (n=8/16)	466.944/n (n=8/16)	245.76/n (n=80/160)	MHz
Ts	Data setup time (min)	5	5	5	5	5	ns
Th	Data hold time (min)	5	5	5	5	5	ns

2.15 I²S - serial audio interface

The SAI serves as 2-stereo channels input/output audio bus interface (e.g. to an external audio- processor, or from an external HD decoder) using the I²S protocol. The latter calls for a bit clock line, a word select line and data lines; the two SAI interfaces on the TDA7706M have both one data input line and one data output line.

There is one audio SAI that uses four lines: SAI_CLK (GPIO8, pin 37) is the bit clock line, SAI_WS (GPIO7, pin 38) is the word select (frame) clock line, SAI_DO (GPIO6, pin 39) is the transmitter output line, SAI_DI (GPIO5, pin 40) is the receiver input line. In master mode SAI_CLK, SAI_WS are outputs, in slave mode these pins are inputs.

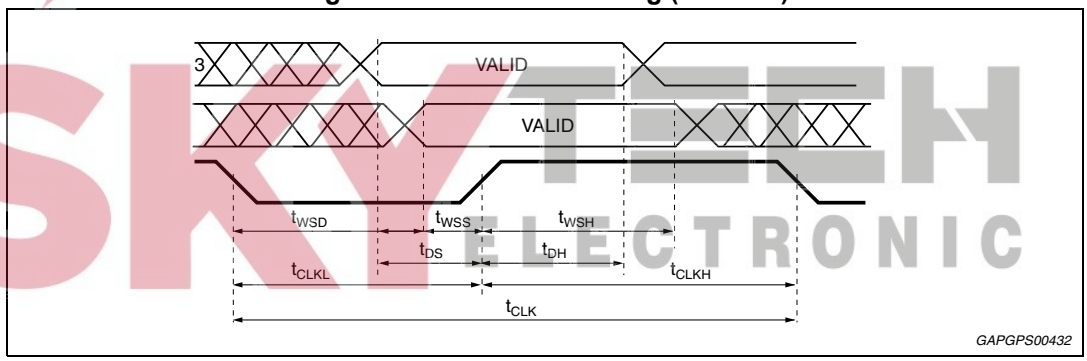
The input and output data lines are operated at the same sampling frequency and of course share the operation mode (master or slave).

The bit clock has one pulse for each discrete bit of data on the data lines. The bit clock operates at a frequency which is a multiple of the sample rate. The bit clock frequency multiplier depends on number of bits per channel, multiplied by the number of channels. In TDA7706M the number of channel is fixed to 2.

Table 8. Audio I²S configuration overview

Name	Channels	World length	Valid Bits	Pins	Formats	Master/Slave mode	Input Rate/ksps	Output Rate /ksps	Max. bit clock frequency	Purpose	Availability
SAI	1x2 In and 1x2 Out	16/24/32	16/24	4	I²S	M/S	32-48	32-48	12.288 MHz	DRM, IBOC, digital audio	64 pin

Figure 8. I²S interface timing (receiver)

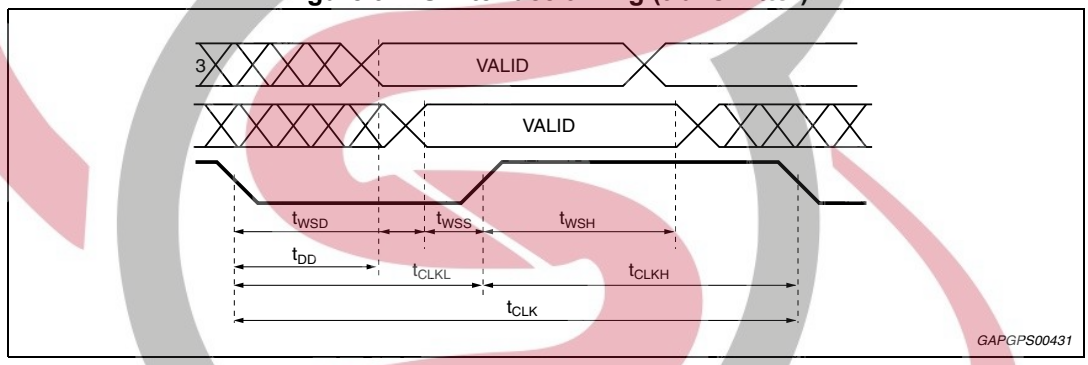


Note: The polarity of the signals and the data bit-shift direction can be selected by configuration bits.

Table 9. I²S interface timing (receiver)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{CLK}	Minimum Clock Cycle (CLK)	-	50	-	-	ns
t_{CLKH}	Minimum bit clock high time	-	25	-	-	ns
t_{CLKL}	Minimum bit clock low time	-	25	-	-	ns
t_{WSS}	Word-select setup time	slave mode	5	-	-	ns
t_{WSH}	Word-select hold time	slave mode	3	-	-	ns
t_{WSD}	Word-select delay	master mode	4	-	-	ns
t_{DS}	Data setup time	-	5	-	-	ns
t_{DH}	Data hold time	-	5	-	-	ns

Figure 9. I²S interface timing (transmitter)



Note: The polarity of the signals and the data shift direction can be selected by configuration bits.

Table 10. I²S interface timing (transmitter)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{CLK}	Minimum Clock Cycle (CLK)	-	50	-	-	ns
t_{CLKH}	Minimum bit clock high time	-	25	-	-	ns
t_{CLKL}	Minimum bit clock low time	-	25	-	-	ns
t_{WSS}	Word-select setup time	slave mode	5	-	-	ns
t_{WSH}	Word-select hold time	slave mode	5	-	-	ns
t_{WSD}	Word-select delay	master mode	5	-	-	ns
t_{DD}	Data delay	-	5	-	-	ns

The SAI can be configured via software to be operating either in master or in slave mode. The frame length is selectable as 16/32 bits per word, with either 16/24 valid bits. *Figure 10* shows the default setting of SAI for the 16-bit mode. Different settings of clock polarity, word clock polarity, transmission mode (I²S mode) and data direction (either MSB or LSB first transmission) are possible, and they can be changed through software. Supported configurations are shown in *Figure 11*. Besides, SAI can be configured to operate in burst mode. Timing information for the protocols is detailed in *Figure 11*.

Figure 10. I²S interface 16-bit

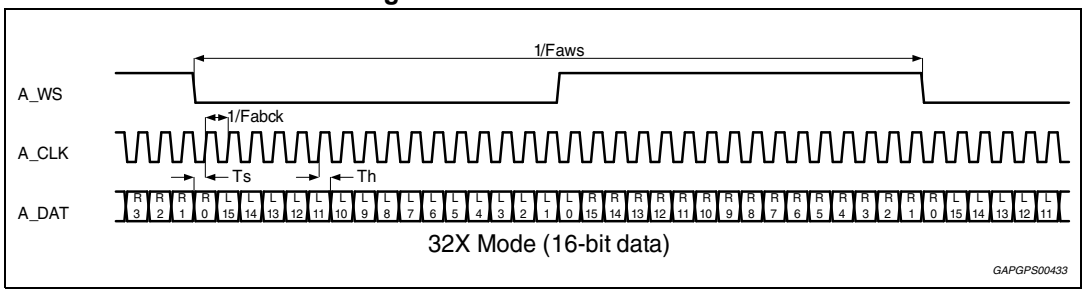
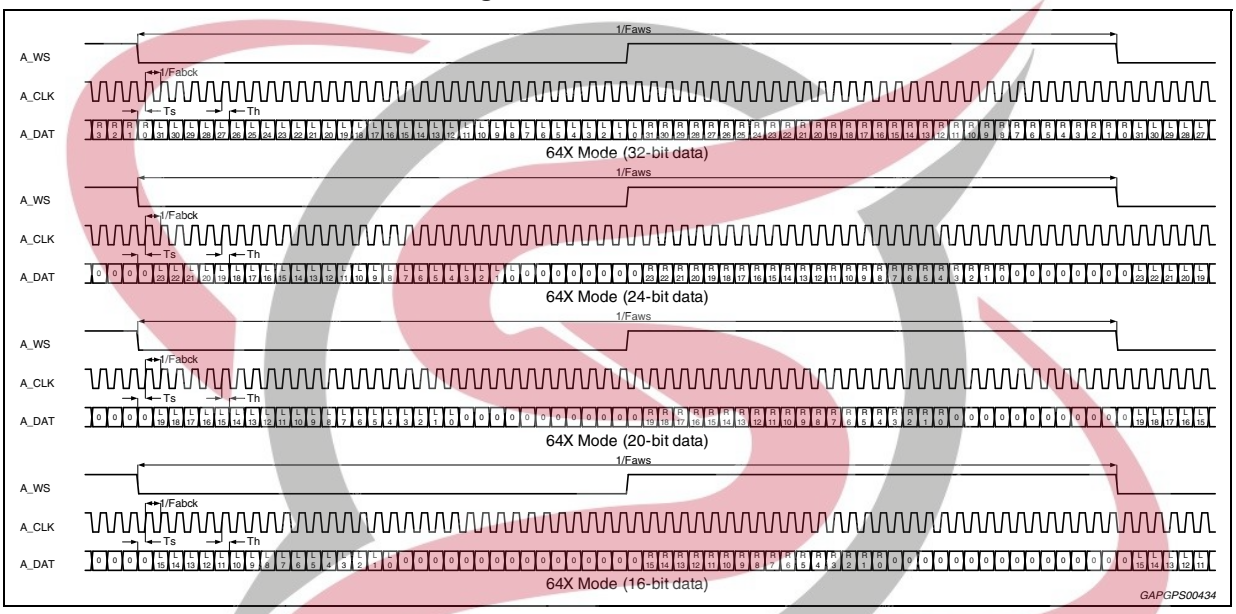


Figure 11. I²S interface 32/24/20/16-bit



2.16 Audio sample rate converter

The sample rate converter block consists of 3 independent sample rate converters (SRC) for stereo input or output. The SRCs are able to convert input frequencies between 32 kHz and 48 kHz to the internal audio processing rate at 45.6 kHz and vice-versa. The bandwidth of the digital input signal must be limited to Fsout/2 in case of down-sample rate (Fsin > Fsout) to get an alias-free output signal. This can be achieved by properly configuring the corresponding LPF channel.

The sample rates needed for the conversion are automatically detected. Each SRC includes a sample clock jitter rejection function which can be enabled separately. The input-signal word-width is 20bits for all 3 SRCs, while the output signal word width can be independently selected as 20 bits or 16 bits.

2.17 Serial control interface

The device is controlled with a standard I²C.

Through the serial bus the processing parameters can be modified and the signal quality parameters and the RDS information can be read out.

The operation of the device is handled through high level commands sent by the main car-radio microprocessor through the serial interface, which allows simplification of the operations carried out in the main microprocessor. The high level commands include among others:

- set frequency (which allows to avoid computing the PLL divider factors);
- start seek (the seek operation can be carried out by the TDA7706M in a completely autonomous fashion);
- RDS seek/search (jumps to AF and quality measurements are automatically sequenced).

2.17.1 Serial interface / boot mode

The device can communicate with the main microprocessor through I^2C. The configuration is chosen by applying the proper voltage at the output from reset at the pins as indicated in *Table 11*. The configuration is latched (e.g. made effective) when the RSTN line transitions from low to high (when RSTN is low, the IC is in reset mode).

The voltage level forced to the boot pins must be released to start the system operation a suitable time after the RSTN line has gone high. The list of configurations is shown in the following table:

Table 11. 64-pin package boot mode configuration

SAI DO pin 39 CONF2	**RDS_INT pin 32 CONF0**	**BOOT mode**	**BUS mode**
0	0	EXT	I^2C slave (Address = 0xC2)
0	1	EXT	I^2C slave (Address = 0xC8)

Two I^2C chip addresses are possible: 0xC2/C3 or 0xC8/C9.

The status of these pins during the reset phase can be set to:

- High: through external <10 kΩ resistors tied to 3.3V
- Low: by not forcing any voltage on them from outside, as 50 kΩ internal pull-down resistors are present inside the device.

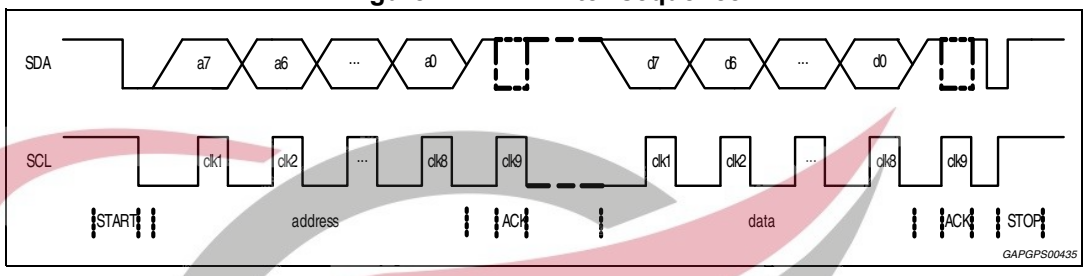
To make sure the boot mode is correctly latched up at start-up, it is advisable to keep the RSTN line low until the IC supply pins have reached their steady state, and further keep it low for an additional time Treset.

2.17.2 I²C bus protocol

The I²C communication requires two signals: clock (SCL) and data (SDA - bidirectional). The protocol requires an acknowledge signal after any 8-bit transmission.

A "write" communication example is shown in the figure below, for an unspecified number of data bytes (see the relevant technical documentation for frame structure description):

Figure 12. I²C "write" sequence

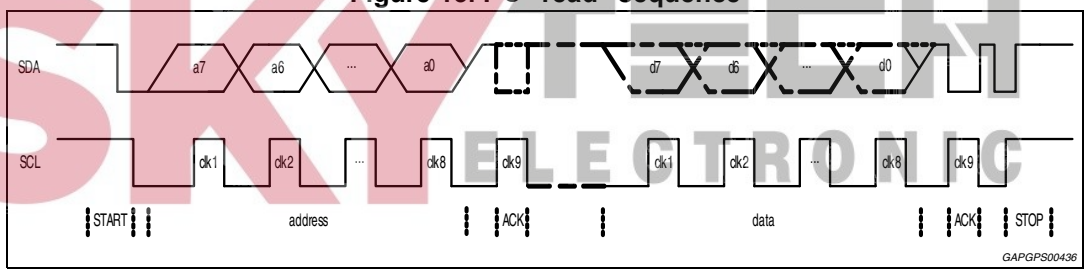


The sequence consists of the following phases:

1. START: SDA line transitioning from H to L with SCL fixed H. This indicates that a new transmission is starting;
2. DATA LATCHING: on the rising SCL edge. The SDA line can vary only when SCL is low (otherwise its transitions are interpreted as either a START or a STOP transition);
3. ACKNOWLEDGE: on the 9th SCL pulse the microprocessor keeps the SDA line H, and the TDA7706M pulls it down in case the communication has been successful. Lack of the acknowledge pulse generation from the TDA7706M indicates a communication failure; the chip-address byte must be sent at the beginning of the transmission. The value can be C2 or C8 (according to the mode chosen at start-up during boot) for "write"; as many data bytes as needed can follow the address before the communication is terminated. See the next section for details on the frame format;
4. STOP: SDA line transitioning from L to H with SCL H. This signifies the end of the transmission.

Dashed lines represent transmissions from the TDA7706M to the microprocessor. A "read" communication example is shown in the figure below, for an unspecified number of data bytes (see later on for frame structure description):

Figure 13. I²C "read" sequence



The "read" sequence is similar to the "write" and it has the same constraints for start, stop, data-latching and the following differences:

The differences follow:

- the chip address must always be sent by the microprocessor to the TDA7706M; the address must be C3 (if C2 had been selected at boot) or C9 (if C8 had been selected at boot);
- the header is transmitted after the chip address (the same happens for "write") before data are transferred from the TDA7706M to the microprocessor. See the relevant technical documentation for details on the frame format;
- when data are transmitted from the TDA7706M to the µP, the latter keeps the SDA line H;
- the acknowledge pulse is generated by the µP for those data bytes that are sent by the TDA7706M to the µP. Failure of the µP to generate an ACK pulse on the 9th CLK pulse has the same effect on the TDA7706M as a STOP.

The maximum clock speed is 500kbit/s.

Warning: When the TDA7706M is not powered on, the internal ESD protection diodes act as a pull-down keeping the I^{2}C lines voltage below 2 V. This implies that the I^{2}C bus connected to the TDA7706M may not be used to drive other devices when the TDA7706M is powered off.

2.18 Digital-down-converter (DDC)

The complex digital mixer in the DDC performs mixing of the IF signal to ZIF (Zero IF). The internal sample rate for FM/AM processing is 456 kS/s and the sample rate for FM/AM IBOC is 912kS/s. AM IBOC and DRM require additional filtering implemented in software.

Figure 14. Digital-down-converter simplified block diagram

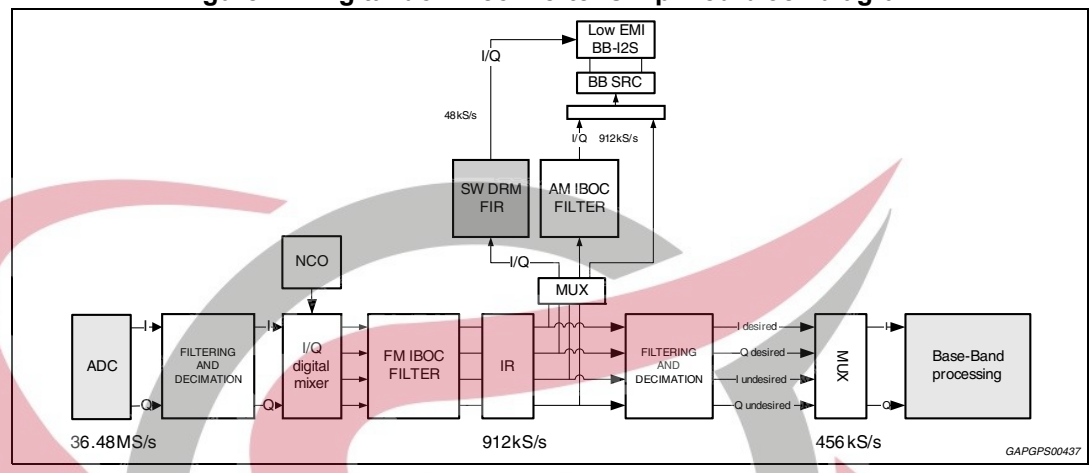


Figure 15. Cumulative transfer function at output of IBOC_FM filter

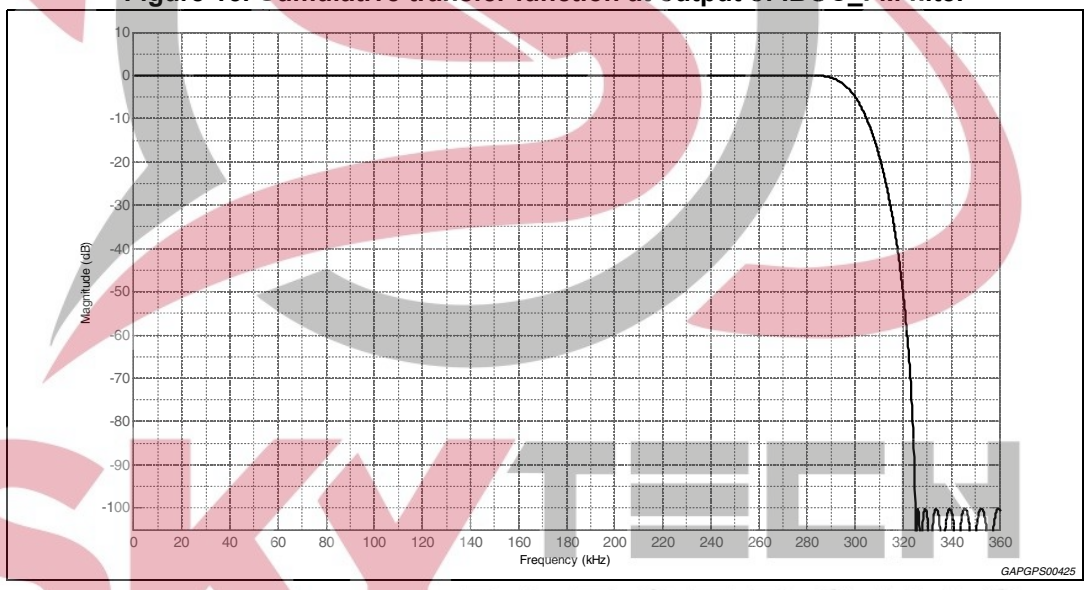


Table 12. Overall filter characteristics for IBOC_FM filter

Item	Value	Unit
Pass-band edge	282	kHz
Stop-band edge	325	kHz
In-band ripple (0kHz to 282kHz)	<0.002	dB
Anti-alias band range	[-500 +500]	kHz
Anti-alias Attenuation	100	dB

Figure 16. Cumulative transfer function at output of IBOC_AM filter

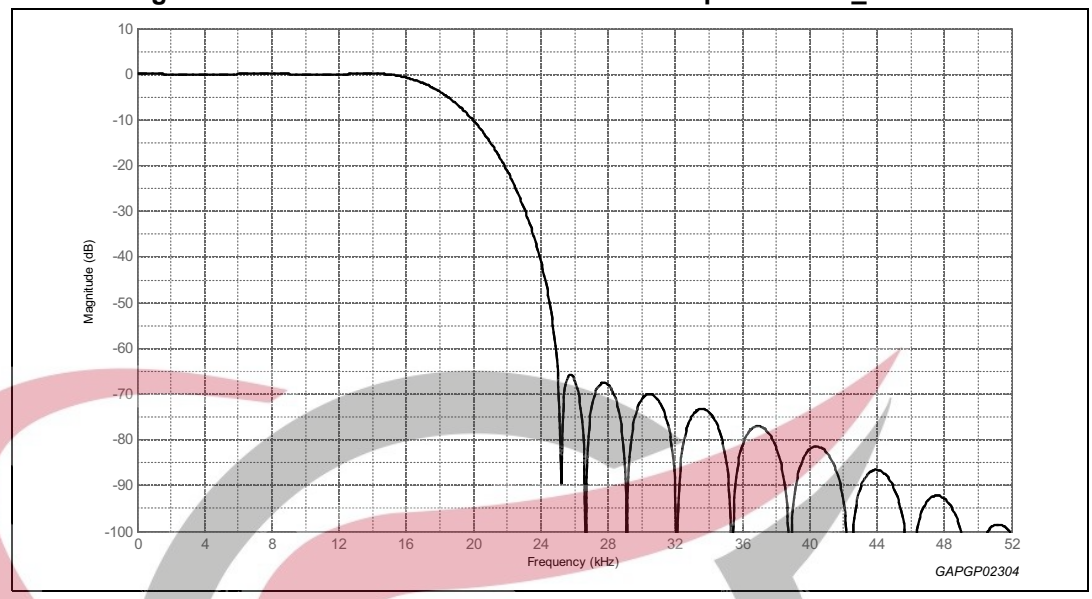


Table 13. Overall filter characteristics at output of IBOC_AM filter

Item	Value	Unit
Pass-band edge	15	kHz
Stop-band edge	25	kHz
In-band ripple	<0.34	dB
Anti-alias Attenuation	>100	dB

Figure 17. Cumulative digital-down-converter transfer function for FM

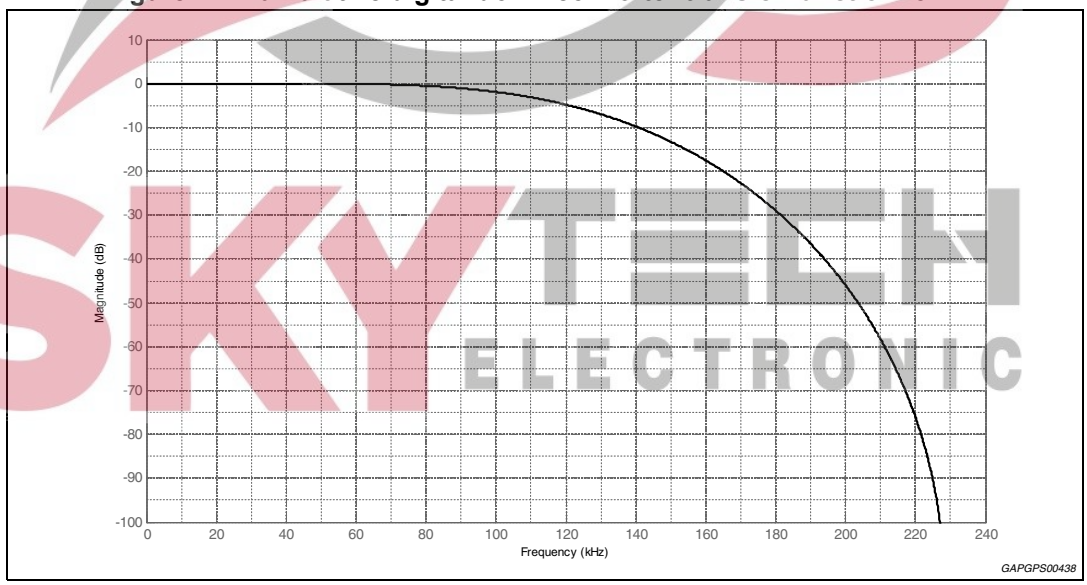


Table 14. Overall filter characteristics for FM (not including DISS filter)

|Item	Value	Unit
Pass-band edge	45.8	kHz
Stop-band edge	228	kHz
In-band ripple	<0.003	dB
Anti-alias Attenuation	>100	dB

Figure 18. Cumulative digital-down-converter transfer function for AM

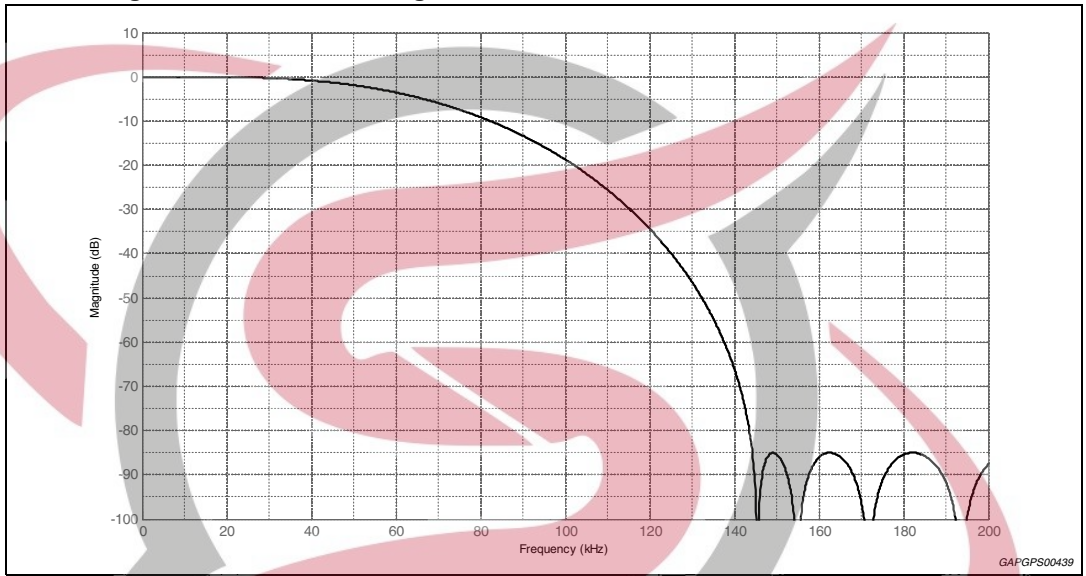


Table 15. Overall filter characteristics for AM

|Item	Value	Unit
Pass-band edge	20	kHz
Stop-band edge	300	kHz
In-band ripple	<0.051	dB
Anti-alias Attenuation	>100	dB

3 Electrical specifications

3.1 Absolute maximum ratings

Table 16. Absolute maximum ratings

Symbol	Parameter	Test condition	Min	Typ	Max	Units
V_{CC}	Abs. supply voltage	-	-0.5	-	5.5	V
T_{stg}	Storage temperature	-	-55	-	150	°C
V_{ESD}	ESD absolute minimum withstand voltage	Human Body model	>|±2000|			V
		Charged device model	>|±400|			
		Charged device mode, corner pins	>|±750|			
-	Max. input at any pin (latch-up characteristic)	I_{INMAX}	±100			mA

Note: For all pins 37-44, when set as input, injecting current cannot exceed 20 mA as it would lead to voltage at the pin above the abs max.

3.2 Thermal data

Table 17. Thermal data

Symbol	Parameter	Test condition	Value	Units
R_{th}	Thermal resistance	LQFP64 10x10, JEDEC 2s1p PCB	55	°C/W

3.3 General key parameters

Table 18. General key parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Units
V_{CC}	5 V supply voltage	-	4.7	5	5.2	V
I_{CC}	supply current @ 5 V	-	-	215	293	mA
T_{amb}	Ambient temperature range	-	-40	-	85	°C
$V_{VCCREG12}$	VCCREG12 supply voltage	see note (1)	2.3	-	5.2	V
V_{1V2}	Digital core 1.2 V supply voltage	when supplied externally see note (2)	1.1	1.2	1.3	V
I_{1V2}	Digital core 1.2 V supply current	V_{1V2} = 1.2V see note(2)	-	75	152	mA
V_{3V3}	Digital IO 3.3 V supply voltage	when supplied externally see note(3)	3.0	-	3.6	V

Table 18. General key parameters (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Units
I_{3V3}	Digital IO 3.3 V supply current	V_{3V3} = 1.2V Maximum current specified only in case generated from Internal supply only	-	-	10	mA

1. In the typical application supplied from 5 V with a 15 Ω series resistor.
   Test condition: maximum current load for minimum value, unloaded for maximum value.
2. When the 1.2 V supply is applied externally, and not using the internal 1.2 V regulator.
   Test condition: FM functional test from antenna mixer input to audio output.
3. When the 3.3 V supply is applied externally, and not using the internal 3.3 V regulator.

3.4 Electrical characteristics

V_{CC} = 4.7 V to 5.25 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified.

3.4.1 FM - section

Table 19. FM - section

Symbol	Parameter	Test condition	Min	Typ	Max	Units
FM IMR Mixer						
RF Gain	Voltage gain (mix in -> s.e. test output)	RF gain 0	33	35	37	dB
		RF gain 1(1)	36	38	40	
		RF gain 2	37	39	41	
		RF gain 3	39	41	43	
Vnoise low gain	Input noise voltage (RF gain 0)	Rsource=1.25kΩ, noiseless	-	2.3	2.9	nV/√Hz
		Rsource=0	-	2.1	2.6	
Vnoise high gain	Input noise voltage (RF gain 3)	Rsource=1.25kΩ, noiseless	-	1.9	2.4	nV/√Hz
		Rsource=0	-	1.6	2.0	
IIP3	3rd order intercept point	RF gain 0, up to Vin/tone = 92 dBµV	124	127	-	dBµV
		RF gain 3, up to Vin/tone = 86 dBµV	119	122		
FM AGC						
RFAGC-Thr	RFAGC threshold, referred to mixer input; RF level	min setting, reg8<14>=1	85.4	88.4	91.4	dBµV
		max setting, reg8<14>=1	89	92	95	
		min setting, reg8<14>=0	88.4	91.4	94.4	
		max setting, reg8<14>=0	92	95	98	
	Threshold steps	-	1.3	1.8	2.3	dB
	Threshold error	@ T_{amb}	-1.5	-	1.5	dB
	Threshold temperature drift	-	-	0.016	-	dB/K

Table 19. FM - section (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Units
IFAGC-Thr	IFAGC threshold	min setting	120	122	124	dBµV
		max setting	126	128	130	dBµV
	Threshold steps	-	1.5	2	2.5	dB
	Threshold error	@ T_{amb}	-1.5	-	1.5	dB
	Threshold temperature drift	-	-	0.016	-	dB/K
Time constant	I attack	Slow attack	10	20	30	µA
		Fast attack	100	200	300	
	I decay	Slow decay	1	2	5	
		Fast decay	10	20	30	
-	PIN diode source current	@ T_{amb} (2)	-15	-	-	mA
-	PIN diode sink current	-	3	-	20	µA
-	PIN diode source current in constant current mode	@ T_{amb}	-0.9	-	-	mA

1. The gain is internally 6 dB more than what measured at the test output. This is due to the differential to single-ended conversion used for the test output.
2. The current is generated by a PTAT (proportional to absolute temperature) source, and has therefore a temperature dependency described by: ΔI/Io = ΔT/To, with Io being the current at ambient temperature (25 °C) and To the ambient temperature (25 °C) expressed in Kelvin, that is 298K.

3.4.2 AM - section

Table 20. AM - section

Symbol	Parameter	Test condition	Min	Typ	Max	Units
AM IMR Mixer						
Gain	Voltage gain (mix in -> s.e. test output)(1)	normal	20	22	24	dB
		reduced	17	19	21	
Rin	Input resistance	-	20	30	45	kΩ
Vnoise	Input noise voltage	Mix 1, 2 R_{source} = 1 kΩ, noise-less	-	7.5	9	nV/√Hz
IIP3	3rd order intercept point	Mix1, 2 up to Vin/tone = 90 dBµV	128	132	-	dBµV
IIP2	2nd order intercept point	Mix1, 2 up to Vin/tone = 90 dBµV	152	158	-	dBµV
LO hsupp	LO harmonic suppression	-	80	-	-	dB
AM LNA						
Gain	Voltage gain	Max gain, R_{ext} = 470 Ω	24	28	32	dB
		Min gain (AGC controlled)	8	12	16	
R_{in}	Input resistance	-	600	950	1300	kΩ
C_{in}	input capacitance	-	-	20	-	pF

Table 20. AM - section (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Units
V_{noise}	Input noise voltage	-	-	0.7	1.0	nV/√Hz
IIP3	3rd order intercept point	@ maximum LNA gain	116	120	-	dBµV
IIP2	2rd order intercept point	@ maximum LNA gain	121	127	-	dBµV
AM PIN diode						
IIP2	2rd order intercept point	Full attenuation, Csource = 80 pF, f=1 MHz	134	140	-	dBµV
Res	Minimum resistance	-	-	5	15	Ω
Cin	Input capacitance	High ohmic	-	2	-	pF
AM AGC						
AGC-Thr	Referred to mixer input; RF level	Mix 1,2 min setting	80	83	86	dBµV
		Mix 1,2 max setting	92.6	95.6	98.6	
Thr-steps	Threshold steps	-	1.3	1.8	2.3	dB
-	Threshold error	@ T_{amb}	-2.5	-	2.5	dB
-	Threshold temperature drift	-	-3	-	3	dB
-	PIN diode source current	@ T_{amb} See note(2)	-10	-	-	mA
-	PIN diode sink current	-	15	30	45	µA
-	PIN diode source current in constant current mode	@ T_{amb} See note(2)	-1	-	-	mA

1. The gain is internally 6 dB more than what measured at the test output. This is due to the differential to single-ended conversion used for the test output.
2. The current is generated by a PTAT (proportional to absolute temperature) source, and has therefore a temperature dependency described by: DI/Io = DT/To, with Io being the current at ambient temperature (25 °C) and To the ambient temperature (25 °C) expressed in Kelvin, that is 298K.

3.4.3 VCO

Table 21. VCO

Symbol	Parameter	Test condition	Min	Typ	Max	Units
$fvco_{,min}$	Minimum VCO oscillation frequency (1)	-	-	-	2.34	GHz
$fvco_{,max}$	Maximum VCO oscillation frequency (2)		3.025	-	-	GHz
PN	Phase noise of LO	Locked VCO; values referred @ 100MHz @ 100 Hz @ 1 kHz @ 10 kHz	-	 -105 -115 -115	-	dBc/Hz
dev	deviation error (RMS)	FM reception, deemphasis 50 µs, f_{audio}=20 Hz...20 kHz	-	5	8	Hz

1. Limited by application Firmware to 2.1 GHz.
2. Limited by application Firmware to 3.1 GHz.

3.4.4 Phase locked loop

Table 22. Phase locked loop

Symbol	Parameter	Test condition	Min	Typ	Max	Units
T_{settle}	Settling time FM	Δf < 10 KHz	-	100	140	µs
FM step	FM Frequency step	-	-	5	-	kHz
AM step	AM frequency step	-	-	500	-	Hz

3.4.5 Tuning DAC

Table 23. Tuning DAC

Symbol	Parameter	Test condition	Min	Typ	Max	Units
R_{es}	Resolution	8 bit	14	18	22	mV
V_{outmin}	Min output voltage	-	-	0.6	0.75	V
V_{outmax}	Max output voltage	-	VCC-0.25	VCC-0.15	-	V
R_{out}	Output impedance	-	1.5	2.5	3.5	kΩ
DNL	Diff. Nonlinearity	-	-	-	0.5	LSB
T_{conv}	Conversion time	Without capacitive load	-	20	-	µs

3.4.6 IF ADC

Table 24. IF ADC

Symbol	Parameter	Test condition	Min	Typ	Max	Units
DR_{FM}	Dynamic range in FM	BW = ±100 kHz	87	90	-	dB
$Vnoise_{FM}$	Input noise referred to mixer input	RF gain 2	1.7	0.94	-	nV/√Hz
DR_{AM}	Dynamic range in AM	BW = ±3 kHz	105	108	-	dB
$Vnoise_{AM}$	Input noise referred to mixer input	normal gain	6.3	3.2	-	nV/√Hz
DR_{FM-HD}	Dynamic range in FM-IBOC	BW = ±200 kHz	82	85	-	dB
$Vnoise_{FM-HD}$	Input noise referred to mixer input	RF gain 2	2.3	1.2	-	nV/√Hz
DR_{AM-HD}	Dynamic range in AM-IBOC	BW = ±15 kHz	97	100	-	dB
$Vnoise_{AM-HD}$	Input noise referred to mixer input	normal gain	5.6	2.9	-	nV/√Hz

3.4.7 Audio DAC

Table 25. Audio DAC

Symbol	Parameter	Test condition	Min	Typ	Max	Units
V_{out}	Max. output voltage	Full scale	1.2	1.4	-	Vrms
BW	Pass-band	0.01dB attenuation	-	20	-	KHz
Rout	Output resistance	-	100	150	200	Ω
onoise	Output noise	-	-	14	30	µVrms
D	Distortion	-6 dBFS	-	0.03	0.05	%

3.4.8 IO interface pins

Table 26. IO interface pins

Symbol	Parameter	Test condition	Min	Typ	Max	Units
-	High level output voltage	Unloaded	2.9	3.2	-	V
-	Low level output voltage	Unloaded	-	0.1	0.3	V
-	Input voltage range	-	0	-	3.5	V
-	High level input voltage	-	2.0	-	-	V
-	Low level input voltage	-	-	-	0.8	V
T_{reset}	Reset time	Minimum time during which pin RSTN must be low so as to reset the device	10	-	-	µs
T_{latch}	Boot mode configuration latch time	Minimum time during which the voltage applied at pins 32 and 39 must be driven in order to latch the correct control serial bus address configuration	10	-	-	µs

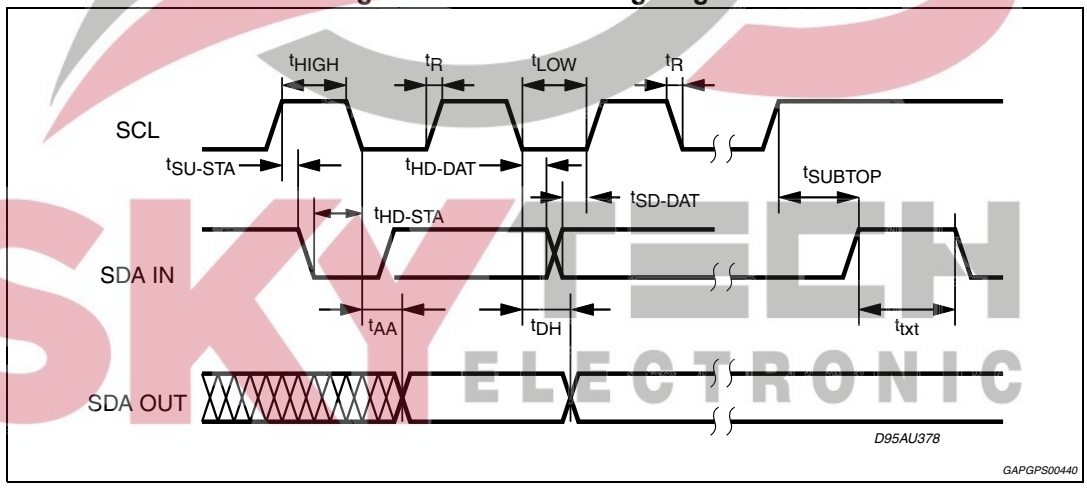
3.4.9 I²C interface

The I²C protocol serial bus communication parameters of the following table are defined as in *Figure 19*.

Table 27. I²C interface

Symbol	Parameter	Test condition	Min	Typ	Max	Units
f_{SCL}	SCL Clock frequency	-	-	-	500	kHz
t_{AA}	SCL low to SDA data valid	-	0.3	-	-	µs
t_{buf}	Time the bus must be kept free before a new transmission	-	1.3	-	-	µs
t_{HD-STA}	START condition hold time	-	0.6	-	-	µs
t_{LOW}	Clock low period	-	1.3	-	-	µs
t_{HIGH}	Clock high period	-	0.6	-	-	µs
t_{SU-SDA}	START condition setup time	-	0.1	-	-	µs
t_{HD-DAT}	Data input hold time	-	0	-	0.9	µs
t_{SU-DAT}	Data input setup time	-	0.1	-	-	µs
t_R	SDA & SCL rise time	-	-	-	0.3	µs
t_F	SDA & SCL full time	-	-	-	0.3	µs
$t_{SU-STOP}$	Stop condition setup time	-	0.6	-	-	µs
t_{DH}	Data out time	-	-	-	0.3	µs

Figure 19. I²C bus timing diagram

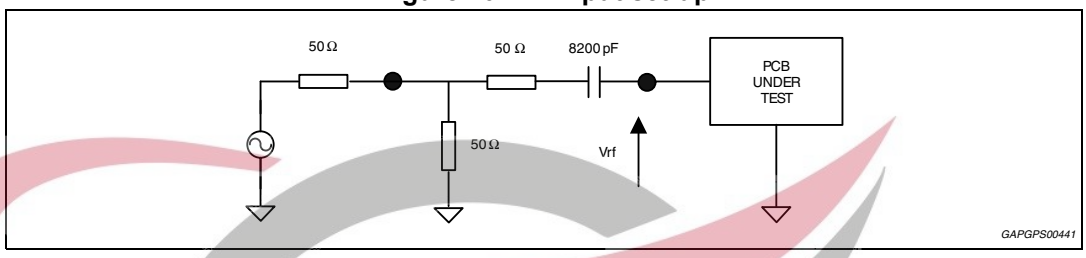


3.5 Overall system performance

3.5.1 FM overall system performance

Antenna level equivalence: 0 dBµV = 1 µVrms (Antenna terminal voltage with 75Ω dummy load).

Figure 20. FM input set-up



Input level referred to 75 Ω antenna dummy output. F_{rf} = 98.1 MHz, V_{rf} = 60 dBµV, mono modulation, f_{dev} = 40 kHz, f_{audio} =1 kHz audio. De-emphasis = 50 µs. Wide-band, not-tuned pre-selection application, unless otherwise specified.

Table 28. FM overall system performance

Parameter	Test condition	Min	Typ	Max	Units
Tuning range FM Eu	(can be modified by the user) (automatic FE alignment available)	87.5	-	108	MHz
Tuning step FM Eu	(can be modified by the user)	-	100	-	kHz
Tuning range FM US	(can be modified by the user) (automatic FE alignment available)	87.5	-	107.9	MHz
Tuning step FM US	(can be modified by the user)	-	200	-	kHz
Tuning range FM Jp	(can be modified by the user) (automatic FE alignment available)	76	-	90	MHz
Tuning step FM Jp	(can be modified by the user)	-	100	-	kHz
Tuning range FM EEu	(can be modified by the user) (automatic FE alignment not available)	65	-	74	MHz
Tuning step FM EEu	(can be modified by the user)	-	100	-	kHz
Sensitivity	S/N = 26 dB	-	-6	-3	dBµV
S/N	@ 10 dBµV, no high-cut, DISS BW = #4	49	52	-	dB
Ultimate S/N	@ 60 dBµV, mono	77	80	-	dB
	@ 60 dBµV, Deviation = 75 kHz, mono	82	85	-	dB
	@ 60 dBµV, stereo	67	70	-	dB

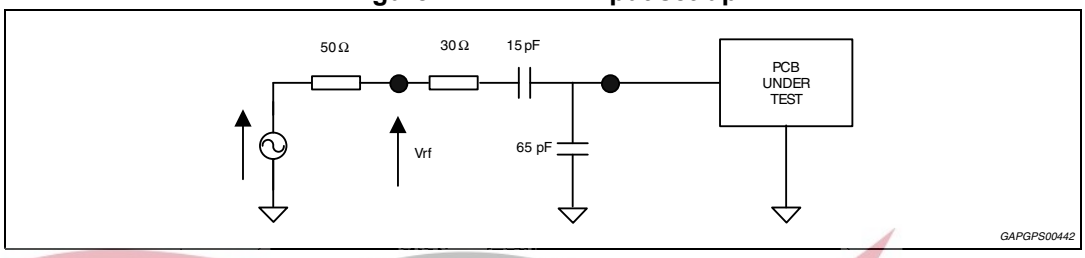
Table 28. FM overall system performance (continued)

Parameter	Test condition	Min	Typ	Max	Units
Distortion	Deviation= 75 kHz	-	0.05	0.1	%
Max deviation	THD=3%	150	166	-	kHz
Adjacent channel Selectivity (D/U ratio)	ΔF=100 kHz, SINAD=30 dB Desired 40 dBµV, dev = 40 kHz, 400 Hz undesired Dev=40 kHz, 1 kHz	20	30	-	dB
Alternate Channel Selectivity (D/U ratio)	ΔF= 200 kHz, SINAD=30 dB Desired 40 dBµV, dev = 40 kHz, 400 Hz undesired Dev=40 kHz, 1 kHz	52	62	-	dB
Max. Strong Signal Interferer (D/U ratio)	Desired = 40 dBµV SINAD = 30 dB Undesired ΔF = 1MHz	75	80	-	dB
3 signal performance (“wide-band”) application	Desired = 40 dBµV, dev = 40 kHz, 400 Hz, SINAD = 30 dB Undesired1 = ± 400 kHz, dev = 40 kHz, 1 kHz Undesired2 = ± 800 kHz, no mod	101	106	-	dBµV
	Desired = 40 dBµV, dev = 40 kHz, 400 Hz, SINAD = 30 dB Undesired1 = ±1 MHz, dev = 40 kHz, 1 kHz Undesired2=±2MHz, no mod	105	110	-	dBµV
AM suppression	m= 30 %	60	70	-	dB
Logarithmic field strength indicator	@40 dBµV read “FM_Smeter_log”	-0.41 (equivalent to 37 dBµV)	-0.38	-0.35 (equivalent to 43 dBµV)	-

3.5.2 AM MW overall system performance

Antenna level equivalence: 0 dBµV = 1 µVrms

Figure 21. AM MW input set-up



Level referred to SG EMF output before antenna dummy; dummy antenna load as shown above F_{rf} = 999 kHz (1000 kHz for US), V_{rf} =74 dBµV, mod = 30 %, f_{audio} =400 Hz, unless otherwise specified.

Table 29. AM MW overall system performance

Parameter	Test condition	Min	Typ	Max	Units
Tuning range MW Eu/Jp	(can be modified by the user)	531	-	1629	kHz
Tuning step MW Eu/Jp	(can be modified by the user)	-	9	-	kHz
Tuning range MW US	(can be modified by the user)	530	-	1710	kHz
Tuning step MW US	(can be modified by the user)	-	10	-	kHz
Sensitivity	S/N = 20 dB	-	25	28	dBµV
Ultimate S/N	@ 80 dBµV	67	72	-	dB
AGC F.O.M.	Ref.=74 dBµV -10dB drop point	(1)	64	-	dB
Distortion	M=80%	-	0.1	0.2	%
Adjacent channel selectivity	ΔF= 9 kHz, SINAD = 26 dB undesired M = 30 %, 1 kHz	44	47	-	dB
Alternate channel selectivity	ΔF = 18 kHz, SINAD = 26 dB undesired M = 30 %, 1 kHz	48	51	-	dB
Strong signal interferer (1) SNR	ΔF= ±40 kHz desired = 40 dBµV undesired = 110 dBµV, m = 30 %, 1 kHz	8	12	-	dB
Strong signal interferer (1) suppression	ΔF= ±40 kHz desired = 40 dBµV undesired = 110 dBµV, m = 30 %, 1 kHz	-	10	15	dB
Strong signal interferer (1) cross-modulation	ΔF= ±40 kHz desired = 80 dBµV undesired = 110 dBµV, m = 30 %, 1 kHz maximum SNR of undesired channel	-	1	4	dB

Table 29. AM MW overall system performance (continued)

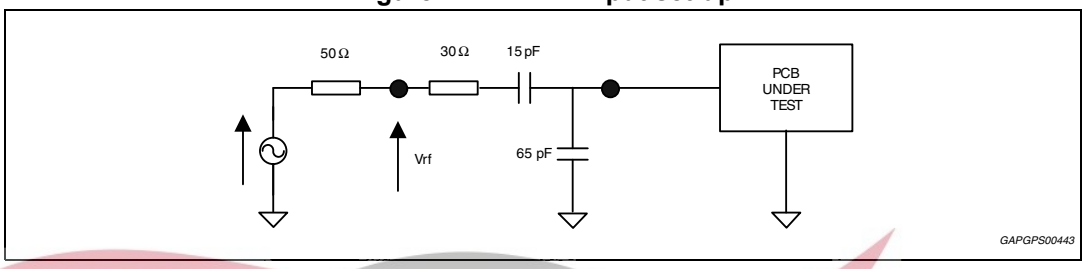
Parameter	Test condition	Min	Typ	Max	Units
Strong signal interferer (2) SNR	ΔF= ±400 kHz desired = 40 dBµV undesired = 110 dBµV, m = 30 %, 1 kHz	5	11	-	dB
Strong signal interferer (2) suppression	ΔF= ±400 kHz desired = 40 dBµV undesired = 110 dBµV, m = 30 %, 1 kHz	-	15	18	dB
Strong signal interferer (2) cross-modulation	ΔF= ±400 kHz desired = 80 dBµV undesired = 110 dBµV, m = 30 %, 1 kHz maximum SNR of undesired channel	-	1	4	dB
Max. strong signal interferer	Desired = 40 dBµV SINAD = 26dB, blocking<6dB Undesired ΔF = 400 kHz, m = 30 % (cross mod. Test)	90	98	-	dBµV
Image rejection	-	60	80	-	dB
Logarithmic field strength indicator	@60 dBµV read "AM_SMeter_log"	-0.47 (equivalent to 57 dBµV	-0.44	-0.41 (equivalent to 63 dBµV)	-

1. Programmable by software parameters.

3.5.3 AM LW overall system performance

Antenna level equivalence: 0 dBµV = 1 µVrms

Figure 22. AM LW input set-up



Level referred to SG EMF output before antenna dummy; dummy antenna load as shown above F_{rf} =216 kHz, V_{rf} =74 dBµV, mod = 30 %, f_{audio} = 400 Hz, unless otherwise specified.

Table 30. AM LW overall system performance

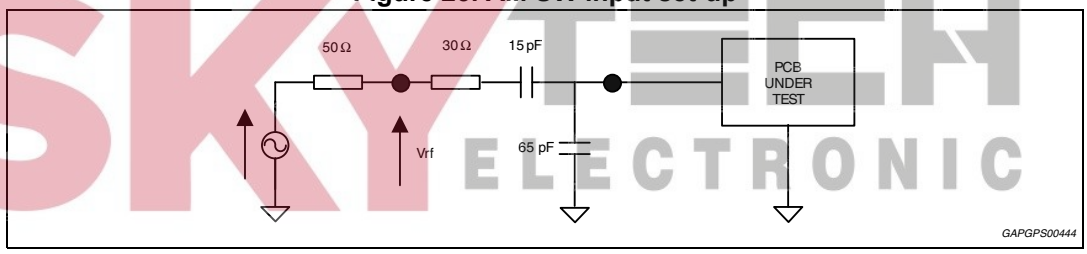
Parameter	Test condition	Min	Typ	Max	Units
Tuning range LW	(can be modified by the user)	144	-	288	kHz
Tuning step LW	(can be modified by the user)	-	1	-	kHz
Sensitivity	S/N =20dB	-	30	34	dBµV
Ultimate S/N	@ 80 dBµV	63	70	-	dB
AGC F.O.M.	Ref. = 74 dBµV -10dB drop point	(1)	64	-	dB
Distortion	M= 80 %	-	0.1	0.2	%
Image rejection	-	60	80	-	dB

1. Programmable by software parameters.

3.5.4 AM SW overall system performance

Antenna level equivalence: 0 dBµV = 1 µVrms

Figure 23. AM SW input set-up



Level referred to SG EMF output before antenna dummy; dummy antenna load as shown above; F_{rf} = 6000 kHz, V_{rf} =74 dBµV, mod = 30 %, f_{audio} = 400 Hz, unless otherwise specified.

Table 31. AM SW overall system performance

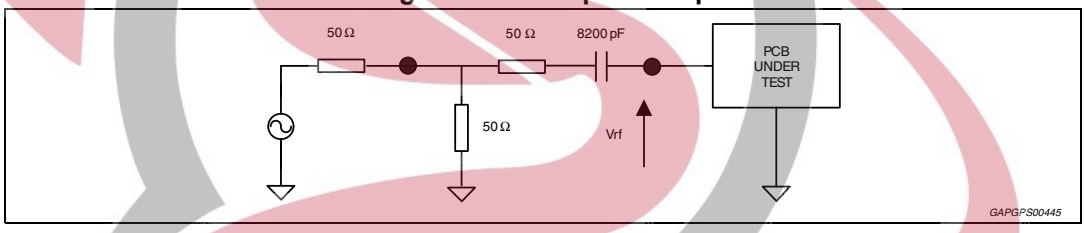
Parameter	Test condition	Min	Typ	Max	Units
Tuning range SW	(can be modified by the user)	2300	-	30000	kHz
Tuning step SW	(can be modified by the user)	-	1	-	kHz
Sensitivity	S/N =20dB	-	26	32	dBµV
Ultimate S/N	@ 80 dBµV	63	70	-	dB
AGC F.O.M.	Ref.=74 dBµV -10dB drop point	(1)	58	-	dB
Distortion	M=80%	-	0.1	0.2	%
Image rejection	-	60	80	-	dB

1. Programmable by software parameters.

3.5.5 WX overall system performance

Antenna level equivalence: 0 dBµV = 1 µVrms (Antenna terminal voltage with 75Ω dummy load).

Figure 24. WX input set-up



Input level referred to 75 Ω dummy antenna output; antenna dummy as shown above. F_{rf} = 162.475 MHz, V_{rf} = 60 dBµV, mono modulation, f_{dev} = 3 kHz, f_{audio} = 400 Hz audio. De-emphasis = 75 µs. Application WX using mixer input 2.Unless otherwise specified.

Table 32. WX overall system performance

Parameter	Test condition	Min	Typ	Max	Units
Sensitivity	S/N = 26 dB	-	-6	-3	dBµV
Ultimate S/N	@ 60 dBµV	70	81	-	dB
Distortion	Deviation= 4.5 kHz	-	0.8	1	%
Max deviation	THD = 3%	5	-	-	kHz
Adjacent channel Selectivity	ΔF= 25 kHz, SINAD = 30dB desired 40 dBµV, dev = 2.0 kHz, 400 Hz undesired Dev = 2.0 kHz, 1 kHz	60	70	-	dB
Alternate Channel Selectivity	ΔF= 50 kHz, SINAD = 30dB desired 40 dBµV, dev = 2.0 kHz, 400 Hz undesired Dev = 2.0 kHz, 1 kHz	60	70	-	dB

4 Front-end registers

All the parameters in this section refer to the programmability of the FE part of the device (registers). The part of the registers that are not described here have either fixed values or values written by the tuner drivers, and are described in the proper technical documentation.

Table 33. Register 0x00

Register number																							Register definition
MSB																						LSB	
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																							AM mixer input selector
																						0	1	Input #1
																						1	0	Input #2
																								AM PIN diode
											0													Internal
											1													External
																								AM AGC mode
										0														LNA and PIN diode
										1														PIN diode only
																								AM AGC time constant
								0	0															Slow (125 ms with 1 µF)
								0	1															Medium (25ms with 1 µF)
								1	1															Fast (5ms with 1 µF)
																								AM AGC thresholds @ mixin
					0	0	0																	90.2 dBµV @ mixin
					0	0	1																	92.0 dBµV @ mixin
					0	1	0																	93.8 dBµV @ mixin
					0	1	1																	95.6 dBµV @ mixin
					1	0	0																	88.4 dBµV @ mixin
					1	0	1																	86.6 dBµV @ mixin
					1	1	0																	84.8 dBµV @ mixin
					1	1	1																	83 dBµV @ mixin
																								AM AGC attack time constant
			0																					Normal
			1																					Fast

Table 34. Register 0x01

Register number																							Register definition
MSB																						LSB	
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																								FM mixer RF-gain
																				0	0			35 dB
																				0	1			38 dB
																				1	0			39 dB
																				1	1			41 dB
																								FM mixer input
									0	1														Input #1 (single-ended)
									1	0														Input #2 (single-ended)
									1	1														Input #1/2 (differential)
																								FM AGC output mode
0	0																							Normal
0	1																							Constant 15mA
1	1																							Constant 1mA

Table 35. Register 0x02

Register Number																							Register Definition	
MSB																					LSB			
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																								FM RF AGCThresholds@ mixin
																						0	0	88.4 dBµV	Reg 0x008<14> = 1
																						0	1	90.2 dBµV	
																						1	0	92.0 dBµV	
																						1	1	93.8 dBµV	
																						0	0	91.4 dBµV	Reg 0x008<14> = 0
																						0	1	93.2 dBµV	
																						1	0	95.0 dBµV	
																						1	1	96.8 dBµV	
																								FM IFAGC threshold@IFADCin	
																				0	0			122 dBµV	
																				0	1			124 dBµV	
																				1	0			126 dBµV	
																				1	1			128 dBµV	
																								FMAGC attack time constant	
																			0					slow	
																			1					fast	
																								FMAGC decay time constant	
																		0						slow	
																		1						fast	
																								FM DAC	
																	0							off	
																	1							on	
																								FM DAC VALUE	
									0	0	0	0	0	0	0	0								0	
									0	0	0	0	0	0	0	1								1	
									…	…	…	…	…	…	…	…								…	
									1	1	1	1	1	1	1	1								255	

Table 36. Register 0x05

Register Number																							Register Definition
MSB																						LSB	
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																								GPODATA
																							0	low
																							1	high

Table 37. Register 0x08

Register number																							Register definition
MSB																						LSB	
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																								FMAGC gain select
									0															FM AGC thresholds high
									1															FM AGC thresholds down

5 Weak signal processing

All the parameters in this section refer to the programmability of the DSP part of the device. The typical values are those set by default parameters (start-up without parametric change from main microprocessor); the max and the min values refer to the programmability range. The values are referred to the typical application ("wide-band" in FM). Wherever the possible values are a discrete set, all the possible programmable values are displayed.

5.1 FM IF-processing

5.1.1 Dynamic channel selection filter (DISS)

Table 38. Dynamic channel selection filter (DISS) - discrete set

Symbol	Parameter	Test condition	Min	Typ	Max	Units
DISS BW	IF filter #6	response: - 3dB	-	±150	-	kHz
	IF filter #5		-	±110	-	kHz
	IF filter #4		-	±80	-	kHz
	IF filter #3		-	±60	-	kHz
	IF filter #2		-	±45	-	kHz
	IF filter #1		-	±35	-	kHz
	IF filter #0		-	±25	-	kHz

5.1.2 Soft mute

Table 39. Soft mute - continuous set

Symbol	Parameter	Test condition	Min	Typ	Max	Units
SMsp	Start point vs. field strength	audio atten = 1 dB read “FM_SoftMute” no adjacent channel present	0	6	20	dBµV
SMep	End point vs. field strength	audio atten = SMd + 1 dB read “FM_SoftMute” no adjacent channel present	-6	-6	10	dBµV
SMd	Depth		-30	-15	0	dB
SMtauatt	Field strength LPF cut-off frequency for soft mute activation		0.1	100	4000	Hz
SMtaurel	Field strength LPF cut-off frequency for soft mute release		0.1	1	4000	Hz

5.1.3 Adjacent channel mute

Table 40. Adjacent channel mute - continuous set

Symbol	Parameter	Test condition	Min	Typ	Max	Units
ACMd	Depth	-	SMd	0	0	dB

5.1.4 Stereo blend

Table 41. Stereo blend - continuous set

Symbol	Parameter	Test condition	Min	Typ	Max	Units
MaxSep	Maximum stereo separation	field strength = 80 dBµV, pilot deviation = 6.75 kHz	0	40	50	dB
SBFSsp	Start point vs. field strength	separation = MaxSep - 1 dB no multipath present	20	50	60	dBµV
SBFSep	End point vs. field strength	separation = 1 dB no multipath present	20	30	60	dBµV
SBFStM2S	Field strength-related transition time from mono to stereo	V_{rf} step-like variation from 20 dBµV to 80 dBµV	0.001	3	20	s
SBFStS2M	Field strength-related transition time from stereo to mono	V_{rf} step-like variation from 80 dBµV to 20 dBµV	0.001	0.5	20	s
SBMPsp	Start point vs. multipath	separation = MaxSep - 1 dB equivalent 19 kHz AM modulation depth; field strength = 80 dBµV	5	10	80	%
SBMPep	End point vs. multipath	separation = 1 dB equivalent 19 kHz AM modulation depth; field strength = 80 dBµV	5	30	80	%
SBMPtM2S	Multipath-related transition time from mono to stereo	V_{rf} step-like variation from 20 dBµV to 80 dBµV	0.001	1	20	s
SBMPtS2M	Multipath-related transition time from stereo to mono	V_{rf} step-like variation from 80 dBµV to 20 dBµV	0.001	0.001	20	s
Pil ThrM2S	Pilot detector stereo threshold	Threshold on pilot tone deviation for mono-stereo transition	0.8	2.74	-	kHz
Pil ThrHyst	Pilot detector threshold hysteresis	Difference in Pil. det. deviation threshold for stereo to mono transition compared to PilThrM2S	-	0.01	-	kHz

5.1.5 High cut control

Table 42. High cut control - continuous set

Symbol	Parameter	Test condition	Min	Typ	Max	Units
HCFSsp	Start point vs. field strength	minimum RF level for widest HC filter (filter # 7) no multipath present	0	50	50	dBµV
HCFSep	End point vs. field strength	maximum RF level for narrowest HC filter (filter # 0) no multipath present	0	30	40	dBµV
HCFStW2N	Field strength-related transition time from wide to narrow band	V_{rf} step-like variation from 60 dBµV to 10 dBµV		(1)		-
HCFStN2W	Field strength-related transition time from narrow to wide band	V_{rf} step-like variation from 0 dBµV to 60 dBµV	(1)	14	100	s
HCMPsp	Start point vs. multipath	minimum RF level for widest HC filter (filter # 7) equivalent 19 kHz AM modulation depth; field strength = 80 dBµV	5	10	150 (2)	%
HCMPep	End point vs. multipath	maximum RF level for narrowest HC filter (filter # 0) equivalent 19 kHz AM modulation depth; field strength = 80 dBµV	5	30	150 (2)	%
HCMPtN2W	Multipath-related transition time from narrow to wide band	V_{rf} step-like variation from 20 dBµV to 80 dBµV	0.001	0.001	20	s
HCMPtW2N	Multipath-related transition time from wide to narrow	V_{rf} step-like variation from 80 dBµV to 20 dBµV	0.001	0.001	20	s
HCmaxBW	Maximum cut-off frequency of high cut filter bank	Filter #7, -3 dB response frequency, input signal with pre-emphasis	HCmin BW	14	18	kHz
HCminBW	Minimum cut-off frequency of high cut filter bank	Filter #0, -3 dB response frequency, input signal with pre-emphasis	0.1	3	HCmaxBW	kHz
HCnumFilt	Number of discrete HC filters	-	-	8 (3)	-	-

1. Depends only on field strength filter time constant.
2. Means that 100% equivalent 19 kHz AM modulation depth will not achieve full band narrowing.
3. Intermediate filters (#6 - #1) cut-off frequencies exponentially spaced between HCmaxBW and HCminBW.

Table 43. De-emphasis filter - continuous set

Symbol	Parameter	Test condition	Min	Typ	Max	Units
DEtc	De-emphasis time constant 1		-	50	-	µs
	De-emphasis time constant 2		-	75	-	

5.1.6 Stereo decoder

Table 44. Stereo decoder - continuous set

Symbol	Parameter	Test condition	Min	Typ	Max	Units
PilSup	Pilot signal suppression	Pilot 9%, 19 kHz, ref=40 kHz	-	60	-	dB
SubcSup	Subcarrier suppression	f = 38 kHz	-	70	-	dB
		f = 57 kHz	-	70	-	dB
		f = 76 kHz	-	80	-	dB

5.2 AM IF-processing

5.2.1 Channel selection filter

Table 45. Channel selection filter

Symbol	Parameter	Test condition	Min	Typ	Max	Units
CSF BW	Channel selection filter BW	response: - 3dB	-	±3.7	-	kHz

5.2.2 Soft mute

Table 46. Soft mute - continuous set

Symbol	Parameter	Test condition	Min	Typ	Max	Units
SMsp	Start point vs. field strength	audio atten = 1 dB read “FM_SoftMute” no adjacent channel present	0	25	40	dBµV
SMep	End point vs. field strength	audio atten = SMd + 1 dB read “FM_SoftMute” no adjacent channel present	0	0	30	dBµV
SMd	Depth		-40	-24	0	dB
SMtauatt	Transition time for field strength-dependent soft mute activation		0.001	0.1	10	s
SMtaurel	Transition time for field strength-dependent soft mute release		0.001	3	10	s

5.2.3 High cut control

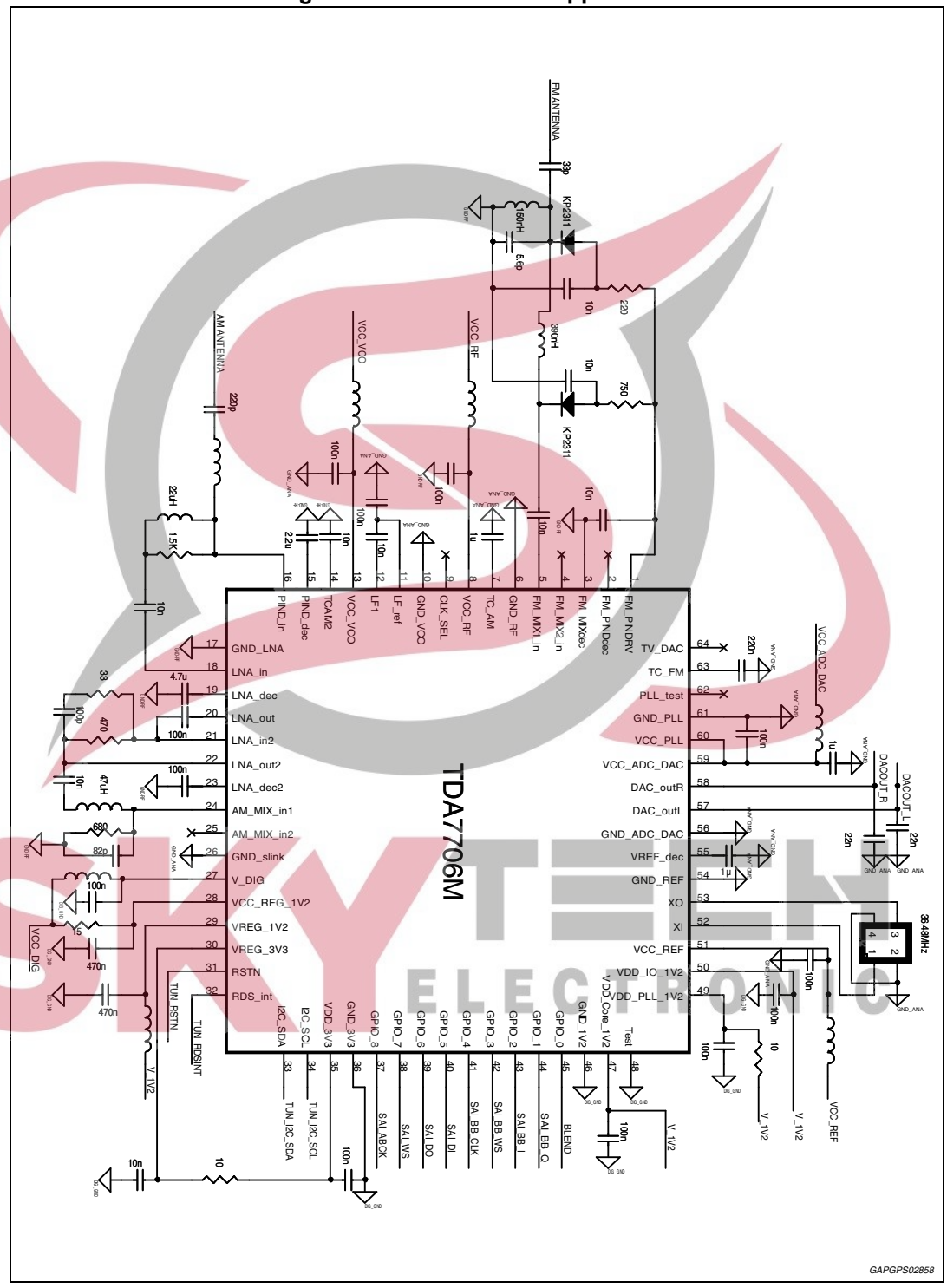
Table 47. High cut control - continuous set

Symbol	Parameter	Test condition	Min	Typ	Max	Units
HCFSsp	Start point vs. field strength	minimum RF level for widest HC filter (filter # 7) no multipath present	0	40	50	dBµV
HCFSep	End point vs. field strength	maximum RF level for narrowest HC filter (filter # 0) no multipath present	0	30	50	dBµV
HCFStW2N	Field strength-related transition time from wide to narrow band	V_{rf} step-like variation from 60 dBµV to 10 dBµV	0.001	0.2	20	s
HCFStN2W	Field strength-related transition time from narrow to wide band	V_{rf} step-like variation from 0 dBµV to 60 dBµV	0.001	10	20	s
HCmaxBW	Maximum cut-off frequency of high cut filter bank	Filter #7, -3 dB response frequency, input signal with pre-emphasis	HCminBW	14	18	kHz
HCminBW	Minimum cut-off frequency of high cut filter bank	Filter #0, -3 dB response frequency, input signal with pre-emphasis	1	3	HCmaxBW	kHz
HCnumFilt	Number of discrete HC filters		-	8	-	-

6 Application schematics

6.1 Basic application schematic

Figure 25. FM wide-band application



7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

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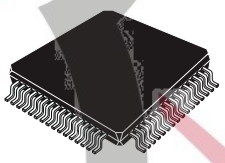
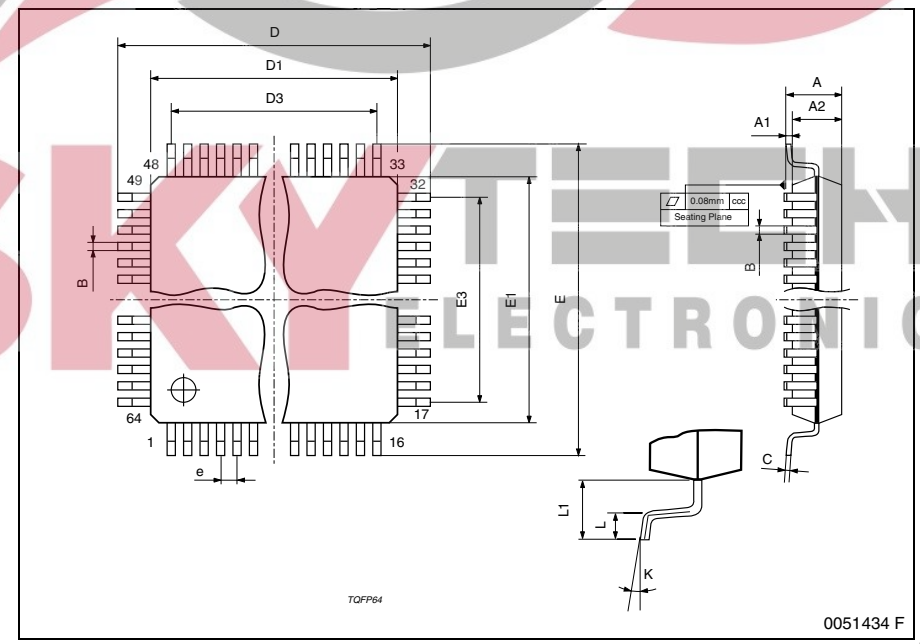
Figure 26. LQFP64 (10x10x1.4mm) mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.0066	0.0086	0.0106
C	0.09		0.20	0.0035		0.0079
D	11.80	12.00	12.20	0.464	0.472	0.480
D1	9.80	10.00	10.20	0.386	0.394	0.401
D3		7.50			0.295	
e		0.50			0.0197	
E	11.80	12.00	12.20	0.464	0.472	0.480
E1	9.80	10.00	10.20	0.386	0.394	0.401
E3		7.50			0.295	
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0393	
K	0° (min.), 3.5° (min.), 7°(max.)					
ccc			0.080			0.0031

OUTLINE AND MECHANICAL DATA



LQFP64 (10 x 10 x 1.4mm)



GAPGPS00365

8 Revision history

Table 48. Document revision history

Date	Revision	Changes
22-Jan-2014	1	initial release.

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